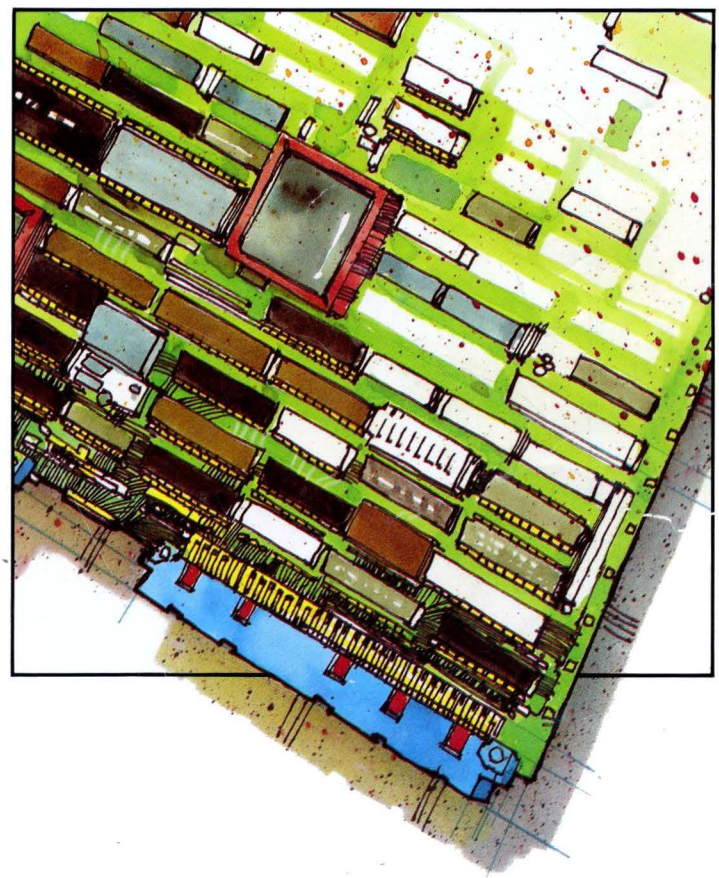
V/SCSI 4210 Jaguar

High-performance VMEbus Dual SCSI Host Adapter

User's Guide



INTERPHASE CORPORATION

V/SCSI 4210
JAGUAR SYSTEM INTERFACE
USER'S GUIDE

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CAUTION

Specific configurations of the V/SCSI 4210 use rows A & C of the connector on P2 for I/O signals. To avoid possible damage to this board, the backplane, or other system components, verify compatibility with the system before installing this board and applying power. (See Appendix A).

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SECTION 1

INTRODUCTION TO THE V/SCSI 4210

OVERVIEW

The V/SCSI 4210 Jaguar is a single or dual SCSI host adapter that can control up to 14 SCSI devices on two separate SCSI physical buses (seven devices per bus). The host processor communicates with the Jaguar through 2048 bytes of dual ported memory that is mapped into the Short I/O space of the VMEbus. All commands and responses pass through this dual ported memory. The system level interface of the V/SCSI 4210 Jaguar is implemented with the Interphase Multiple Active Command Software Interface (MACSI).

This document describes the MACSI of the V/SCSI 4210 Jaguar. The MACSI System Interface of the Jaguar allows the host not only to have multiple commands queued but also for the Jaguar to have multiple commands active simultaneously. The Jaguar accepts commands from the host and queues them internally. It then acts on each command as soon as possible within the confines of the SCSI bus. As commands are completed, the host is notified of both the completion of the command and the status of the completion.

Each command to the Jaguar is fully specified using a software structure that is generated by the host, called an Input/Output Parameter Block (IOPB). The host submits commands to the Jaguar by making an entry into a circular queue called a Command Queue. Each entry in the Command Queue is called a Command Queue Entry (CQE). Each CQE is a 12-byte block containing a pointer to the IOPB and various control information.

To issue a command, the host first builds the IOPB in an area of the Short I/O space specifically reserved for use by the host. It then puts a CQE into the next available slot in the Command Queue. The Jaguar reads the Command Queue and places the control information from the CQE and the IOPB for that particular command into one of another set of internal structures called work queues. After the CQE and the IOPB have been placed in a work queue, the slot in the Command Queue that was filled by the command becomes available for re-use by the host. The Jaguar then automatically performs commands from the work queue at the first opportunity.

When a command is complete, the control information and the IOPB are written by the Jaguar into the Command Response Block, (also located in Short I/O) and an interrupt to the host is generated. The Command Response Block provides completion status and other information that enable the host to identify which command has completed. The host acknowledges the interrupt by writing a word to the Command Response Block which then releases it for further use.

The Command Queue has slots for a number of CQEs. In addition, a CQE occupies a slot in the Command Queue for a very short time (until it is moved into a work queue). As a result, the host virtually always has slots available in the Command Queue for issuing commands. Thus, the host need not be concerned with any of the intimate timing issues of the Jaguar's Command Queue. Even in the unlikely case that the Command Queue is full when the host tries to enter a command, the Jaguar provides efficient operation by optionally interrupting the host when a slot becomes available in the Command Queue.

The concept of work queues is integral to the way that MACSI allows multiple commands to be active simultaneously. Information in the CQE determines the work queue into which a particular command is placed. The various work queues can be prioritized so that commands in one queue take precedence over commands in another queue. Commands from queues of equal priority are started in a round robin fashion. At any time, there is an In Progress command for each work queue that has at least one entry. The Next command is simply waiting for the In Progress command from that work queue to complete.

Since the SCSI bus allows many tasks to be overlapped on multiple devices, the MACSI interface allows for commands from all work queues to be interspersed. Assuming that the SCSI devices support overlapped activity on the SCSI bus (using Disconnect/Reconnect), up to 14 commands (one In Progress command from each attached SCSI device) can be simultaneously active, resulting in overlapped data streams. Indeed, since the Jaguar has two fully independent SCSI buses, it can support two truly simultaneous data streams. If some devices do not support overlapped activity, they can be relegated to the second port, allowing fully functioning devices on the first port unrestricted operation. The second port can, of course, also support full SCSI functionality.

The Jaguar accommodates up to 14 work queues, not counting a special queue called Work Queue 0 (detailed later). Each work queue is initialized separately and may, therefore, have its own properties. The only restriction is that commands for different devices not be mixed in the same work queue. The number of slots in the Command Queue, the number of slots in each work queue, the characteristics of these queues, as well as other Jaguar operating parameters, are programmable and must be initialized before use. In order to accommodate this initialization, and to provide for certain very

high priority functions, the Jaguar, on power-up, provides special facilities called the Master Command Entry and Work Queue 0. The Master Command Entry location in Short I/O space takes exactly the same form as the CQE (with control information and a pointer to an IOPB) and acts like a single slot Command Queue. Likewise, Work Queue 0 is simply a single slot work queue. Using these auto-initialized facilities, a user can issue single commands and wait for their completion before issuing the next one. Normally, the first command sequence would initialize the rest of the queues and start off "normal" operations. The Master Command Entry and Work Queue 0 are not removed even after the Command Queue and the other work queues are initialized and normal activity has begun.

The Master Command Entry and Work Queue 0 also have another important attribute; namely they have the highest possible priority. Any entry made into the Master Command Entry or Work Queue 0 is acted upon before commands in the Command Queue or in any other work queue.

Reference

ANSI X9.3131 - 1968 *Standard for Small Computer Systems Interface*

VME Bus Specification, Revision C.1

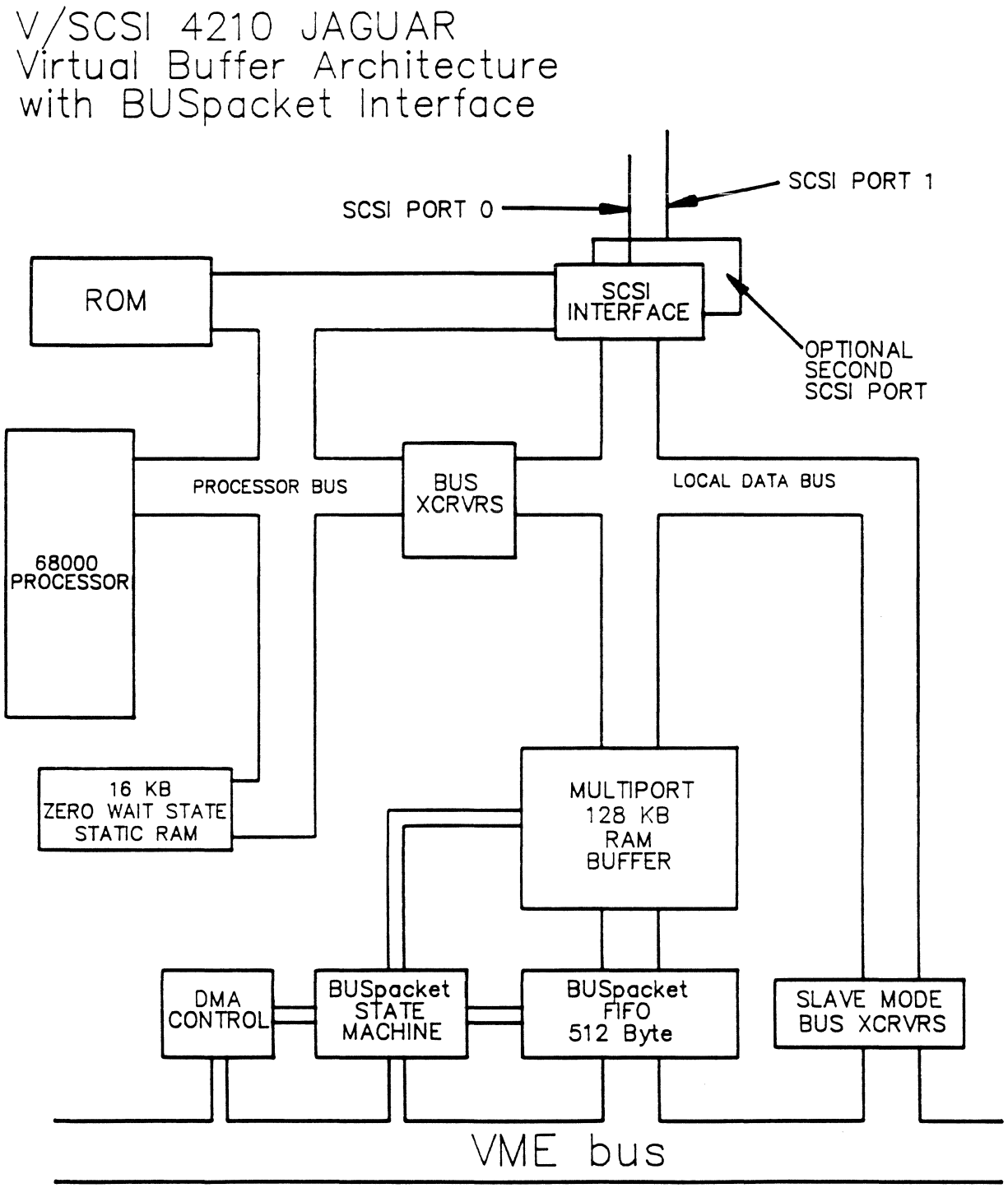


Figure 1. V/SCSI 4210 Jaguar Block Diagram

SECTION 2

JAGUAR SYSTEM INTERFACE DETAILED DESCRIPTION

OVERVIEW

The host communicates with the Jaguar through 2048 bytes of dual ported memory located on the Jaguar. This memory is mapped into the Short I/O space of the VMEbus. Every location can be both written to and read from, physically, by the host at any time, but the protocol of the Jaguar MACSI System Interface puts some restrictions upon when certain areas should be accessed. Also, some areas are logically write only or read only. MACSI partitions this RAM into six major sections:

Master Control/Status Block (MCSB)

Master Command Entry (MCE)

Command Queue (CQ)

Host Usable Space (HUS)

Command Response Block (CRB)

Controller Specific Space (CSS)

The Master Control/Status Block (MCSB) is used to pass and receive information relative to the overall operation of the Jaguar. The Master Control/Status Block is 16 bytes long.

The Master Command Entry (MCE) is used to issue commands to the Jaguar before the Command Queue and work queues have been initialized. Typically, it will be used only when initializing the Command Queue and work queues. It does, however, provide a mechanism to issue a command to the Jaguar even if the Command Queue and all work queues are full. The single slot of the MCE has the same 12-byte format as any other Command Queue entry. Space **must** be reserved in the Host Usable Space (HUS) portion of the dual ported memory for the IOPB that is pointed to by the MCE.

The Command Queue (CQ) consists of a programmable number of slots for Command Queue Entries (CQE). Each CQE includes all of the information that is needed for the host to find, execute, and respond to the commands contained in an IOPB. The CQ is circular, and it is up to the host to keep track of the next CQE that it can use. Because the queue is circular, the Jaguar infers chronological ordering of commands. Each CQE is "busy" only until the Jaguar can transfer the command to a work queue and then free its slot in the CQ. This mechanism allows a large number of commands to be queued up without needing an excessive number of slots in the CQ itself. The number of slots in the CQ are programmed via the INITIALIZE CONTROLLER command. The actual size of the CQ equals the number of slots times 12 bytes. In the Jaguar, the CQ can have a maximum of 40 slots.

The Host Usable Space (HUS) is free-form memory space accessible to both the host and the controller. It is typically used for IOPBs. However, for multiprocessing applications, this is a convenient place for semaphores between CPUs. The amount of HUS available is determined by the number of Command Queue slots defined when the CQ is initialized and by the length of the Command Response Block. For example, if the Command Queue is initialized with 10 slots and the Command Response Block of 76 bytes is defined, there will be 1704 bytes of HUS available. The Master Control/Status Block, Master Command Entry, and the Controller Specific Space always occupy a total of 148 bytes.

The Command Response Block (CRB) is used by the Jaguar to post completion status in two situations: either as a response to a command completion or a queue slot available condition. If the posting is the result of an IOPB completion, the IOPB itself and related status information are returned to the CRB. The offset of the CRB is defined during initialization. The length of the CRB can be determined by subtracting the CRB offset from the offset of the Controller Specific Space (0x788). However, the length of the CRB **must** be equal to the largest IOPB defined plus 12 bytes. A recommended minimum value is 76 bytes.

The Controller Specific Space (CSS) is used by the Jaguar to post the Controller Configuration Status Block. The Jaguar uses the Controller Configuration Status Block to report the firmware revision level, information on product number and variations, available buffer space and the SCSI bus IDs that it is using. The CSS is 120 bytes long.

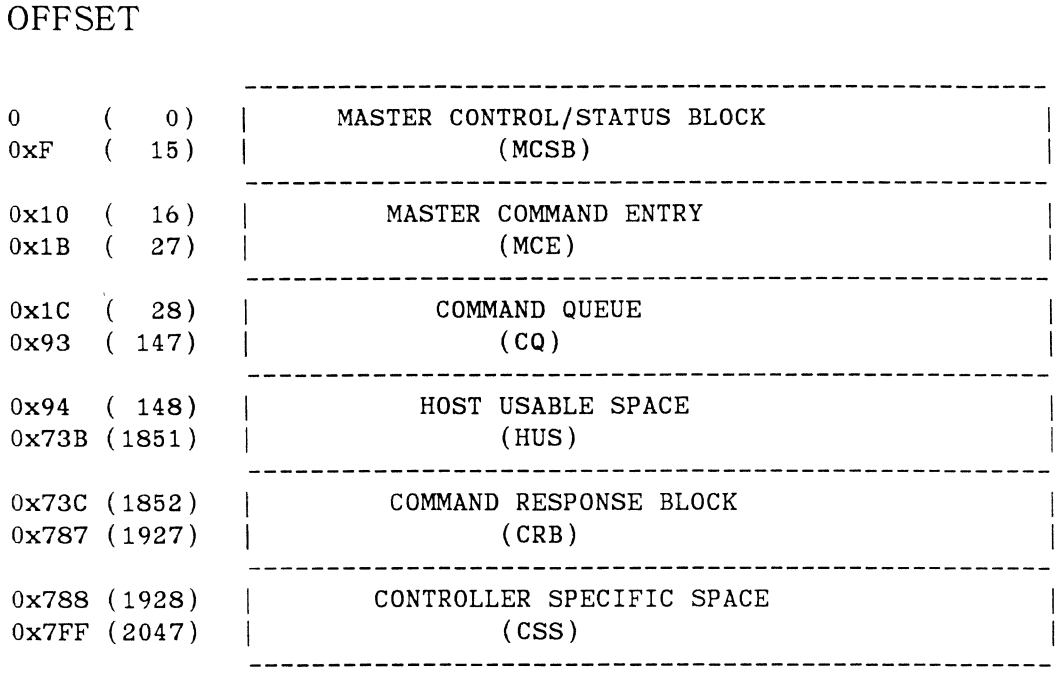


Figure 2. Example Jaguar System Interface Memory Map.

NOTE

This memory map is for a Jaguar that has been initialized with a 10-slot Command Queue and a maximum IOPB length of 64 bytes.

MASTER CONTROL/STATUS BLOCK (MCSB)

The Master Control/Status Block (MCSB) consists of the Master Status Register (MSR), the Master Control Register (MCR), the Interrupt on Queue Available Register (IQAR), and the Queue Head Pointer (QHP).

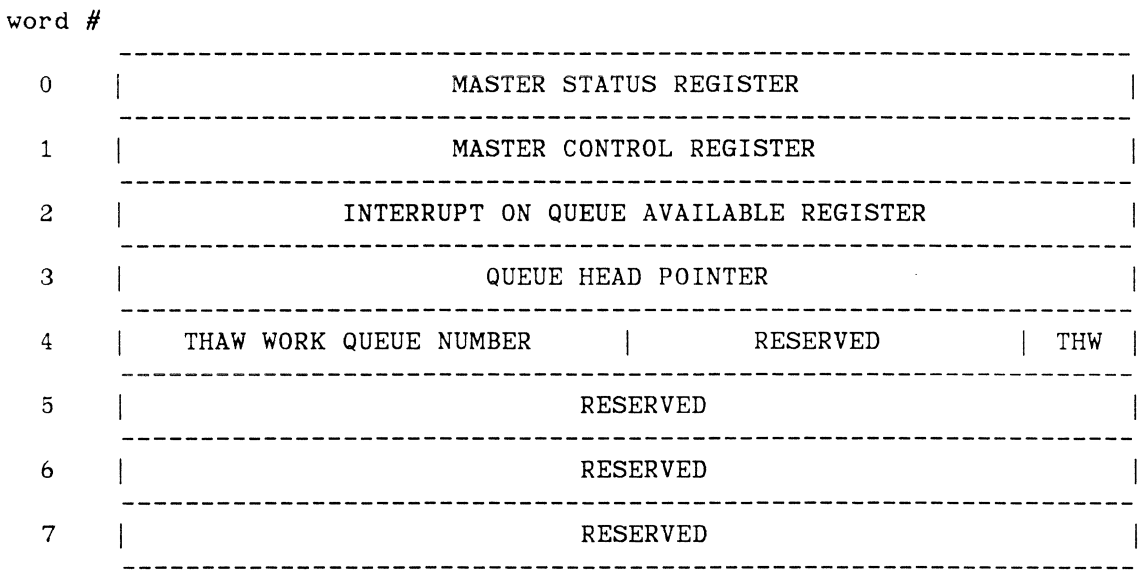


Figure 3. Master Control/Status Block (MCSB)

MASTER STATUS REGISTER (MSR)

The Jaguar uses this register to report board level status. From the host point of reference, this is a READ ONLY register. However, the contents of this register are not valid for 100 microseconds following a controller reset. The bits are defined as follows:

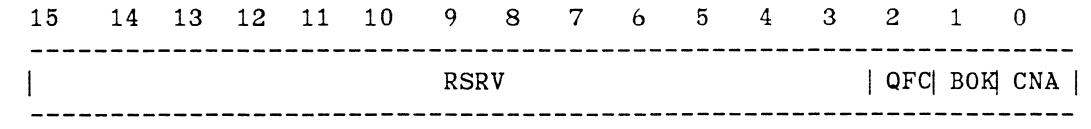


Figure 4. Master Status Register (MSR)

Bit 0 Controller Not Available (CNA):

The Jaguar sets this bit to '1' to indicate that it is Not Available to receive a command. This condition can be caused either by a controller reset or by the execution of controller diagnostics. CNA will also be set if a board initialization command fails to complete (see Initialize Controller Command). The Jaguar will reset this bit to '0' when it is capable of accepting a command.

Bit 1 Board O.K. (BOK):

The Jaguar sets this bit to '1' when the power-up diagnostics are completed successfully. A '0' indicates that the Jaguar detected a failure during the power-up diagnostics or during a board initialize command. The BOK bit is not valid for 100 microseconds after a controller reset.

BOK	CNA	DESCRIPTION
0	0	The controller has failed to operate and is not capable of accepting a command.
0	1	Controller is Not Available. If the controller is not still executing power-up diagnostics, then it has either failed to execute power-up diagnostics correctly or it has failed to complete a board initialize command.
1	1	The controller has successfully completed power-up diagnostics but it is not capable of accepting a command, because it is executing the diagnostics command.
1	0	The controller has completed diagnostics and is capable of receiving commands.

Figure 5. Board OK/Controller Not Available Relationship

Bit 2 Queue Flush Complete (QFC):

The QFC bit is set to '1' by the Jaguar after it performs a flush queue operation. It is cleared by the Jaguar after the Flush Queue bit in the Master Command Register is cleared by the host (see MCR bit descriptions under Master Control Register for more detail).

Bits 3-15 Reserved (RSRV):

These bits are reserved and are set to '0' by the Jaguar.

MASTER CONTROL REGISTER (MCR)

All bits in this register are both set and reset by the host. From the Jaguar's point of reference, this is a READ ONLY register. The Jaguar will never set any of these bits. The bits are defined as follows:

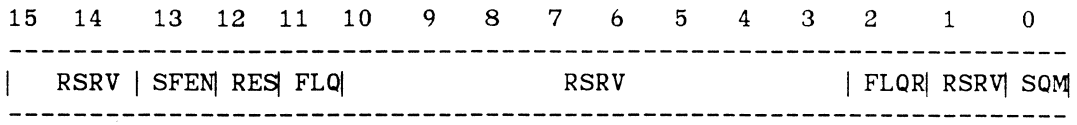


Figure 6. Master Control Register (MCR)

Bit 0 Start Queue Mode (SQM):

Until the Command Queue and work queues are initialized, all commands to the Jaguar must be issued to Work Queue 0 through the Master Command Entry. Once the Command Queue and work queues have been initialized, the host starts Queued IOPB operation by setting this bit to '1'. The host sets this bit only after it has initialized both the Command Queue and the work queues. This bit is set only once by the host and is never reset during normal operation. The Jaguar will acknowledge entering Queued IOPB mode by issuing a Command Complete Interrupt with the Queue Mode Started bit in the Command Response Status Word set to '1' (see Command Response Status Word). The interrupt will use the Controller Interrupt Vectors, which also should be initialized before setting Start Queue Mode (see Initialize Controller Command).

Bit 1 Reserved (RSRV):

This bit is reserved and must be set to '0' by the host.

Bit 2 Flush Queue and Report (FLQR):

The Flush Queue and Report bit causes the Jaguar to clear all In Progress commands and all queued commands from both the Command Queue and the work queues. Any In Progress (currently executing) command will be cleared. If the command has already been sent to a SCSI device, then Flush Queue and Report will reset the SCSI bus also. (Individual work queues can be cleared using the Flush Work Queue command.)

As each command is cleared, a Command Complete Interrupt (with error completion status) is generated. At the completion of the entire Flush Queue and Report operation, a final Command Complete Interrupt is generated. This final Command Complete Interrupt uses the Controller Interrupt Vector. When this interrupt is generated, the Queue Flush Complete bit (QFC) will be set in the Master Status Register. The host should clear the Flush Queue and Report bit before clearing this last interrupt. The host must wait for this final Flush Queue and Report Command Complete Interrupt before entering any new commands, because the Jaguar will continue flushing commands until there are no further commands to flush. Thus, any command entered before the Flush Queue and Report Command Complete Interrupt will be flushed.

Bits 3-10 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

Bit 11 Flush Queue (FLQ):

Flush Queue operates the same as Flush Queue and Report except that there is no report (Command Complete Interrupt) as each command is flushed. A Flush Queue generates only one Command Complete Interrupt at the completion of the entire operation. The Controller Interrupt Vector Register is used for the Command Complete Interrupt. The host must wait for the Flush Queue Command Complete Interrupt before entering new commands, because the Jaguar will continue flushing commands until there are no further commands.

Bit 12 Reset Controller (RES):

The Reset Controller bit controls the microprocessor hardware reset line. It also causes a RESET on both of the SCSI buses. Obviously, it should be used only to recover from extreme error conditions. To ensure proper operation, the host must leave this bit set for at least 50 microseconds.

Bit 13 Sysfail Enable (SFEN):

The Sysfail Enable bit enables the Jaguar to drive the Sysfail signal on the VMEbus if it detects an internal failure during power-up diagnostics. If this bit is '0', the Jaguar will not drive the Sysfail signal under any circumstances.

Bits 14-15 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

INTERRUPT ON QUEUE AVAILABLE REGISTER (IQAR)

The Command Queue is a circular queue with slots for numerous Command Queue Entries (CQE). Each CQE occupies a slot in the Command Queue for a short period of time (until it is moved into a work queue), thus the host will virtually always have slots available in the Command Queue for issuing commands. In the unlikely event that the Command Queue is full when the host attempts to enter a command, the host must wait until the Jaguar transfers a command from the Command Queue to an internal work queue before it can enter the next command.

The host determines that the Command Queue is full by looking at the Go bit in the next available Command Queue Entry. The Command Queue is full if the Go bit of the next available CQE is '1'. If the Command Queue becomes full, the host could simply poll the Go bit, waiting until the next CQE becomes available. But the Jaguar, through the Interrupt on Queue Available Register, provides for efficient operation by optionally interrupting the host when a slot becomes available in the Command Queue. Thus, even in the unlikely case that the Command Queue is full when the host tries to enter a command, the host need not be concerned with any intimate timing issues of the Jaguar's Command Queue.

The Interrupt on Queue Available is enabled by setting the Interrupt on Command Queue Available bit in the Interrupt on Queue Available Register (IQAR). If the Interrupt on Queue Half Empty Enable bit is also set, the Jaguar will not interrupt until the Command Queue is half empty. Otherwise, the interrupt will occur as soon as the Jaguar detects one empty slot in the Command Queue. The host should wait until encountering the Queue Full condition before setting the IQEA bit. Once the IQEA bit is set, the Jaguar generates an interrupt as soon as the necessary queue conditions are satisfied. Once the interrupt is generated, the Jaguar resets the IQEA bit.

The level and vector for the IQEA interrupt are supplied by the host in the IQAR. When the necessary queue conditions are satisfied, the Jaguar clears the IQEA bit and generates a Command Complete Interrupt with the Queue Entry Available (CQA) bit set in the Command Response

Status Word (CRSW) of the Command Response Block (CRB) (see Command Response Status Word). Even though the Jaguar provides for efficient operation by providing this mechanism for interrupting the host when a slot (or slots) become available in the Command Queue, it is preferable for the number of slots in the Command Queue to be set during initialization so that the full condition occurs infrequently (see Initialize Controller Command).

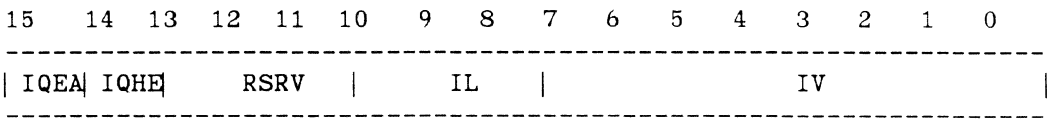


Figure 7. Interrupt on Queue Available Register (IQAR)

Bits 0-7 Interrupt Vector for the Interrupt on Queue Available (IV):

The Jaguar uses this byte as the interrupt vector when issuing an Interrupt on Queue Available interrupt. This byte is set by the host and is not modified by the Jaguar. The host must not modify this byte after setting the IQEA bit.

Bits 8-10 Interrupt Level for the Interrupt on Queue Available (IL):

These three bits determine the interrupt level that the Jaguar will use when issuing an Interrupt on Queue Available interrupt. These bits are set by the host and are not modified by the Jaguar. After setting the Interrupt on Queue Entry Available bit, Bit 15, the host must not modify these bits.

Values of '0' through '7' are allowed. An interrupt level of '0' is allowed only when the IQEA bit is reset.

Bits 11-13 Reserved (RSRV):

These bits must be set to '0' by the host.

Bit 14 Interrupt on Queue Half Empty Enable (IQHE):

This bit is a flag which causes the Jaguar to generate the Interrupt on Queue Available interrupt when the Command Queue becomes half empty (rather than as soon as one slot becomes available). The Interrupt on Queue Half Empty Enable (IQHE) bit is valid only when the IQEA bit is set. The IQHE bit is set by the host and is not modified by the Jaguar. The host must not modify this bit after it has set the IQEA bit.

Bit 15 Interrupt on Queue Entry Available (IQEA):

This bit is set by the host to request an Interrupt on Queue Entry Available. The interrupt is generated either when the queue is half empty or as soon as one slot is available, depending upon the state of the IQHE bit. The Jaguar resets this bit prior to generating the Interrupt on Queue Available interrupt. After the host sets this bit, requesting an interrupt, it cannot change any of the other bits in the Interrupt on Queue Available Register.

QUEUE HEAD POINTER

The Command Queue is a circular queue and the Jaguar requires that the host use the slots in the Command Queue in order. The Queue Head Pointer provides a convenient method for the host to control the ordering of and the access to the Command Queue. The Queue Head Pointer register provides a place for the host to store the address of the next available slot in the Command Queue.

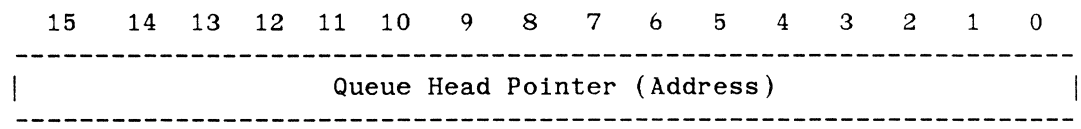


Figure 8. Queue Head Pointer/Queue Head Pointer In Use

Bits 0-15 Queue Head Pointer (Address):

This is the address of the next slot in the Command Queue. Since the Jaguar transfers commands out of the Command Queue in circular order as soon as it sees the Go bit set, this address is not actually used by the Jaguar.

The MACSI interface of the Jaguar relies on the chronological order of the Command Queue. The host must somehow ensure that the slots in the Command Queue are used in chronological order.

THAW WORK QUEUE NUMBER

This register is used to restart a work queue that has been frozen after an error has occurred with Freeze Work Queue on Error enabled. See Appendix C for a complete description of SCSI command error handling.

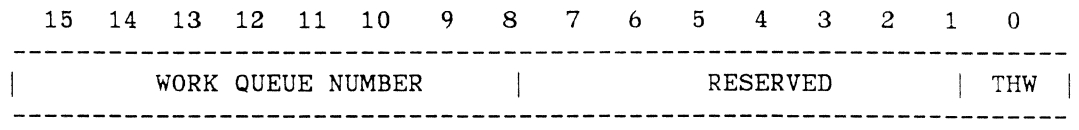


Figure 9. Thaw Work Queue Register

Bit 0 Thaw Work Queue (THW):

Setting this bit causes the Jaguar to resume execution of commands in the work queue specified in Bits 8-15. The Jaguar resets this register to acknowledge thawing the work queue.

Bits 1-7 Reserved:

These bits are reserved and must be set to '0' by the host.

Bits 8-15 Work Queue Number:

This byte specifies the work queue to be unfrozen. This value must not change while Bit 0, THW, is set to '1'.

MASTER COMMAND ENTRY (MCE)

The Master Command Entry (MCE) is used to issue commands to the Jaguar before the Command Queue and work queues have been initialized. Until the Jaguar has been commanded to enter Queue Mode, all commands must be entered through the MCE. Typically, it will be used only when initializing the Command Queue.

It does, however, provide a mechanism to issue a command to the Jaguar even if the Command Queue and all work queues are full. It provides a way to get one command into the Jaguar even when the Command Queue is "locked up."

The single slot of the MCE has the same 12-byte format as any other Command Queue entry. And it is used exactly the same as a "normal" slot in the Command Queue. **For the MCE to be used, space must be reserved in the Host Usable Space (HUS) portion of the dual ported memory for the IOPB pointed to by the MCE.**

COMMAND QUEUE

The Command Queue (CQ) consists of a programmable number of slots for Command Queue Entries (CQE). The number of slots for CQEs in the Command Queue is set by the host when it initializes the controller. The Command Queue is circular, but it is up to the host to keep track of the next Command Queue Entry that it can use. Because the queue is circular, the Jaguar can infer chronological ordering of commands. The actual size of the Command Queue equals the number of slots times 12 bytes. The Jaguar Command Queue can have a maximum of 40 slots.

COMMAND QUEUE ENTRY (CQE)

Each CQE includes all of the information that is needed for the host to find and execute the command contained in an IOPB. Each slot in the Command Queue is "busy" only until the Jaguar can transfer the command to a work queue and then free the slot in the Command Queue. This mechanism allows a large number of commands to be queued up without needing an excessive number of slots in the Command Queue itself. Each CQE consists of a Queue Entry Control Register, an IOPB Address, a Command Tag, a Work Queue Number, and two reserved bytes. Each entry is 2 bytes long, except the Command Tag which is 4 bytes long; thus, there are 12 bytes in each CQE.

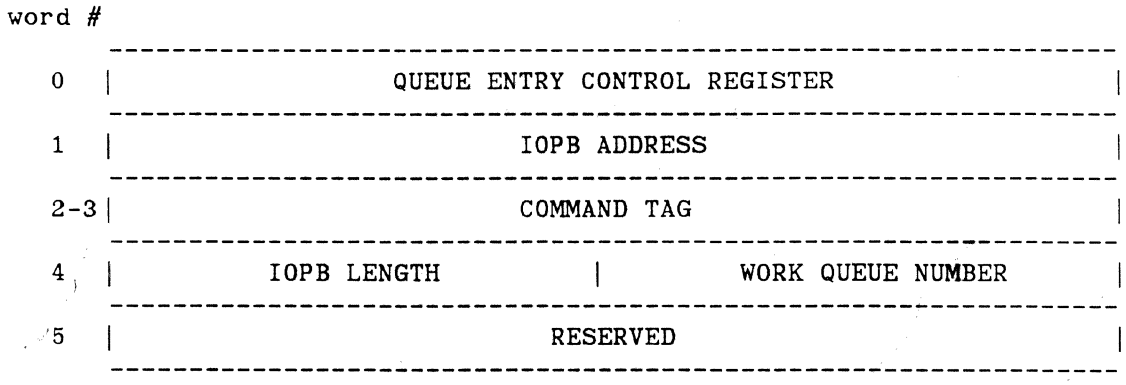


Figure 10. Command Queue Entry

QUEUE ENTRY CONTROL REGISTER (QECR)

The Queue Entry Control Register (QECR) is used to kick off command execution, to request the end of a command abort sequence, and to flag high priority commands. The Queue Entry Control Register is 2 bytes long.

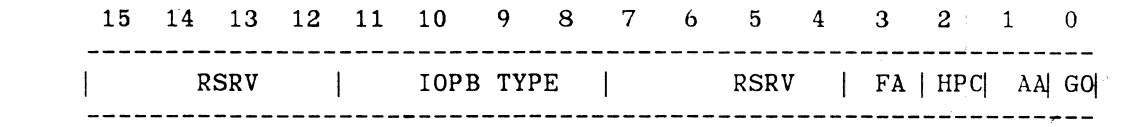


Figure 11. Queue Entry Control Register (QECR)

Bit 0 Go/Busy (GO):

The Go/Busy bit is set by the host to initiate action on a CQE. The host must assemble the IOPB in the Host Usable Space (HUS) and assemble the entire CQE in the Command Queue before it sets this bit. The Jaguar moves the CQE and the IOPB into internal memory as soon as it sees the Go/Busy bit set. Once the IOPB and CQE are in internal memory, the Jaguar will reset the Go/Busy bit to free the slot in the Command Queue.

Bit 1 Abort Acknowledge (AA):

When work queues are initialized by the host, all commands in the queue can optionally be aborted after a command completes with an error (see Initialize Work Queue Command). The Abort Acknowledge bit is the mechanism used as a flag to **stop** aborting commands after this condition occurs.

When Abort on Error is enabled, the Jaguar will abort all commands in the work queue. The Jaguar will also abort all commands in the Command Queue that are destined for that work queue until it finds a command with the AA bit set. Therefore, when a command completes with error, a likely scenario is for the host to re-issue the command that completed in error (with the Abort Acknowledge bit set). Upon successful completion, the host can then re-issue each command that was aborted because of the error (these commands should **not** have the Abort Acknowledge bit set).

Bit 2 High Priority Command (HPC):

The High Priority Command (HPC) bit flags a command so that the Jaguar places the command at the top of its work queue. If there are already other commands in the work queue with the HPC bit set, the new command is queued up directly behind the other High Priority Commands. (Thus, there is a FIFO-type ordering of High Priority Commands.)

Bits 3-7 (RSRV) Reserved:

These five bits are reserved and must be set to '0' by the host.

Bits 8-11 IOPB Type:

These bits describe the IOPB type. The Jaguar supports only type zero IOPBs.

Bits 12-15 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

IOPB ADDRESS

The IOPB Address is a 2-byte pointer to the IOPB associated with the Command Queue Entry. It is the offset of the IOPB from the first location of the dual ported memory. The IOPB must reside in the Short I/O. Since the Jaguar transfers both the CQE and the IOPB into internal memory as soon as it sees the Go/Busy bit set, this section of Short I/O is only "tied up" for a very short time.

COMMAND TAG

The Command Tag is a 4-byte value that the host can use to keep track of individual commands. The Jaguar does not use the Command Tag, nor does it modify it. It simply returns the Command Tag as part of the Command Response. Thus, in a typical implementation, the host would use a unique value Command Tag for each CQE so that it can always differentiate one command from another. The format of the Command Tag is determined solely by the host.

IOPB LENGTH/WORK QUEUE NUMBER

The Work Queue Number byte specifies into which work queue a command (CQE and IOPB) is to be queued. The IOPB Length byte specifies the length of the IOPB itself. A recommended value is 64 bytes.

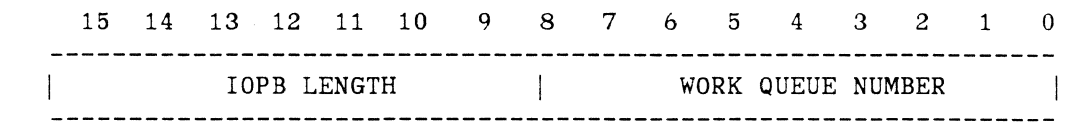


Figure 12. IOPB Length/Work Queue Number

Bits 0-7 WORK QUEUE NUMBER:

Each command (CQE and IOPB) is placed in the work queue specified by the Work Queue Number. The Jaguar supports 14 work queues plus Work Queue 0, for a total of 15 work queues. Before any work queue, except Work Queue 0, is used to queue commands, it must be initialized by the host. (See Initialize Work Queue Command). If the specified work queue has not been initialized, the command will be reported as completing with an error.

Work Queue 0 is a special queue that is auto-initialized by the Jaguar as a single slot queue. This default length of Work Queue 0 cannot be changed by the host. Work Queue 0 is also the highest priority work queue, so any command sent to Work Queue 0 is executed immediately.

The Jaguar places no restrictions on the use of any work queue. The host fixes each work queue's length and priority relative to other work queues during initialization. The host is then responsible for using the work queues in a manner that is consistent with the initialization scheme.

Prior to initialization of the work queues, all commands must be sent through Work Queue 0. Work queues can be reinitialized (see Initialize Work Queue Command).

Bits 8-15 IOPB LENGTH:

The IOPB Length byte specifies the length, in words, of the IOPB that is pointed to by the CQE. An IOPB Length byte of zero indicates that the IOPB is the default length of 0x16 words.

HOST USABLE SPACE (HUS)

The Host Usable Space (HUS) is freeform memory space accessible to both the host and the controller. No partitioning of the HUS is implied or required by the Jaguar MACSI interface. The manner in which it is used is totally under the control of the host. Typically, the HUS in the Jaguar is used to pass the IOPB portion of a command. In some multiprocessing applications, the HUS is a handy place to post semaphores between CPUs.

The amount of HUS available is determined by two factors: the number of Command Queue slots defined when the Command Queue is initialized, and by the length of the Command Response Block that is defined. For example, if the Command Queue is initialized with ten slots (each CQE slot is 12 bytes long) and a Command Response Block of 76 bytes is defined, there will be

1704 bytes of HUS available. The Master Control/Status Block, Master Command Entry, and the Controller Specific Space always occupy a total of 148 bytes.

COMMAND RESPONSE BLOCK (CRB)

The Command Response Block (CRB) is used by the Jaguar to post completion status and data that results from a command completion or from a queue slot available condition. The CRB is made up of the Command Response Status Word (CRSW), the Command Tag, the Work Queue Number, and the Returned IOPB. If the posting is the result of an IOPB completion, the IOPB itself and related status information are returned here.

The offset of the CRB is defined at initialize time. The length of the CRB can be determined by subtracting the Command Response Block offset from the offset of the Controller Specific Space (0x788). However, the length of the Command Response Block **must** be equal to the largest IOPB defined plus 12 bytes. A recommended value for the CRB length is 76 bytes. This would make the offset 0x73C.

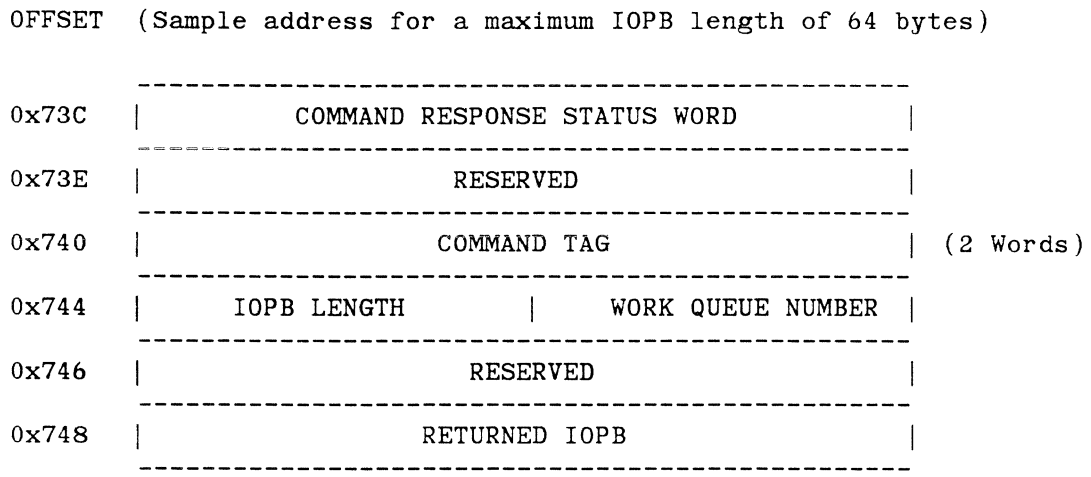


Figure 13. Command Response Block (CRB)

NOTE

The above is the address map of the Command Response Block if the maximum IOPB length is 64 bytes.

COMMAND RESPONSE STATUS WORD (CRSW)

The Command Response Status Word (CRSW) is the first word in the Command Response Block (CRB). It describes the nature of the Command Response. It also contains a Handshake bit and the Command Response Block Valid/Clear Interrupt (CRBV) bit. (The CRBV synchronizes the command interaction of the Jaguar and the host.) The bits of the CRSW are defined as follows:

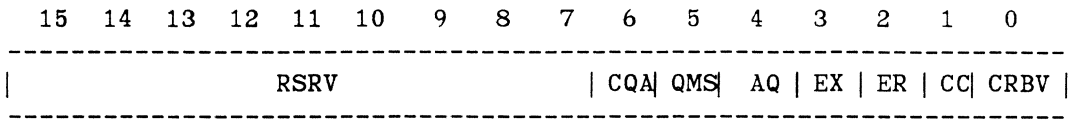


Figure 14. Command Response Status Word (CRSW)

Bit 0 Command Response Block Valid/Clear Interrupt (CRBV):

The Command Response Block Valid/Clear Interrupt (CRBV) bit is set by the Jaguar after it loads the returned IOPB, the Work Queue Number, and the Command Tag into the Command Response Block (CRB).

The CRBV bit is also an **Interrupt Pending** bit because the Jaguar sets it immediately prior to issuing a Command Complete interrupt to the host. The Jaguar keeps the CRB stable while this bit is set.

After it is finished using the information in the CRB, the host clears the interrupt by clearing the CRBV bit. Once this bit is reset, the Jaguar can use the Command Response Block to present the next command response.

Bit 1 Command Complete (CC):

The Command Complete (CC) bit is set by the Jaguar when the Command Response Block is being used to post the response to a Command Completion, as opposed to a Queue Entry Available condition or a Start Queued Mode operation. The CC bit is set even when the command is completed with error or exception. (See Command Response Status Word (CRSW) bits 2 and 3.)

Bit 2 Error (ER):

The Error (ER) bit is set by the Jaguar when the Command Response Block is being used to post a Command Completion with an Error. The host can determine the exact nature of the error by examining the returned IOPB. The Error bit is valid only when Command Complete is active.

Bit 3 Exception (EX):

The Exception (EX) bit is set by the Jaguar when the Command Response Block is being used to post a Command Completion with an Exception. The host can determine the exact nature of the exception by examining the returned IOPB. The Exception bit is valid only when Command Complete is active.

Bit 4 Abort Queue (AQ):

When work queues are initialized by the host, they can be set up (optionally) so that all of the commands in the queue can be aborted after a command completes with an error. (See Initialize Work Queue

Command.) The command that was completed with an error is reported just like any other error, with the Error bit set in the Command Response Status Word.

With Abort on Error enabled, the Jaguar, on an error, will abort all commands in the work queue. In addition, all commands in the Command Queue destined for that work queue will be aborted until a command with the Abort Acknowledge bit set in the Queue Entry Control Register is encountered. (See Queue Entry Control Register). All of the aborted commands are reported in the Command Response Block with the Command Complete, Error, and Abort Queue bits set. The Error Interrupt Vector of the command being aborted will be used to report this condition.

Bit 5 Queue Mode Started (QMS):

The Queue Mode Started (QMS) bit is set by the Jaguar in response to the host setting the Start Queue Mode (SQM) bit in the Master Control Register. (See Master Control Register).

Once the Command Queues and work queues have been initialized, the host starts Queued IOPB operation by setting the SQM bit in the Master Control Register. The Jaguar acknowledges entering Queued IOPB mode by issuing a Command Complete Interrupt with the QMS bit set in the Command Response Status Word. The interrupt will use the Controller Interrupt Vectors, which should also be initialized before setting Start Queue Mode. (See Initialize Controller Command).

Bit 6 Command Queue Entry Available (CQA):

The Command Queue Entry Available (CQA) bit is set by the Jaguar when the Command Response Block is presented in response to a queue entry available condition. The CQA bit is mutually exclusive with the Command Complete bit.

Bits 7-15 Reserved (RSRV):

These bits are reserved and are set to '0' by the Jaguar.

COMMAND TAG

This Command Tag is the same 4-byte value that was provided in the Command Queue Entry when this command was originally issued to the Jaguar. The Jaguar does not use the Command Tag, nor does it modify it. It simply returns the Command Tag as part of the Command Response. The Command Tag is used by the host to determine to which command the Jaguar is responding.

IOPB LENGTH/WORK QUEUE NUMBER

The lower byte of this word specifies the number of the work queue to which the command was issued. The upper byte specifies the length of the returned IOPB. An IOPB Length byte of zero indicates the IOPB is the default length of 0x16 words. The entire IOPB Length/Work Queue Number word is returned from the Command Queue Entry exactly as it was originally entered by the host. It is unchanged by the Jaguar.

RETURNED IOPB

The Returned IOPB field of the Command Response Block is usually an image of the IOPB that was passed with the Command Queue Entry when the command was originally issued to the Jaguar. In some cases, depending upon the specific IOPB, some of the parameters are modified to reflect Command Completion status.

This returned IOPB area is undefined for a response to a Queue Entry Available condition or for any other command response where the original command did not require an IOPB.

CONTROLLER SPECIFIC SPACE

The Jaguar uses the Controller Specific Space (CSS) to post the Configuration Status Block. The CSS is 120 bytes long.

CONTROLLER CONFIGURATION STATUS BLOCK

The Controller Configuration Status Block is used by the Jaguar to report the hardware and firmware configuration in the 120-byte Controller Specific Space. This includes the firmware revision level, information on product number and variations, available buffer space, and the SCSI bus IDs that it is using. Below is the format of the Controller Configuration Status Block.

OFFSET		
0x788	RESERVED	
0x78A	RESERVED	PRODUCT CODE
0x78C	PRODUCT CODE	
0x78E	RESERVED	
0x790	RESERVED	PRODUCT VARIATION
0x792	RESERVED	
0x794	RESERVED	FIRMWARE REVISION LEVEL
0x796	FIRMWARE REVISION LEVEL	
0x798	RESERVED	
0x79A	FIRMWARE RELEASE DATE	
0x7A2	RESERVED	
0x7A4	SIZE OF BUFFER	
0x7A6	RESERVED	
0x7AA	PRIMARY BUS ID	SECONDARY BUS ID
0x7AC	RESERVED (86 BYTES)	

Figure 15. Controller Configuration Status Block

Following is a description of the values found in the Controller Configuration Status Block.

Product Code (3 bytes):

These three bytes are the Interphase product code. This value is represented as a 3-character ASCII string. The most significant character appears first. It is valid after the completion of a controller reset.

Product Variation (1 byte):

This byte is the Interphase product variation code. This value is represented as one ASCII character. This value is valid after the completion of a controller reset.

Firmware Revision Level (3 bytes):

These three bytes are the revision level of the installed firmware. This value is represented as a 3-character ASCII string. The most significant character appears first. This value is valid after the completion of a controller reset.

Firmware Release Date (8 bytes):

These 8 bytes are the release date of the installed firmware. This value is represented as an 8-character ASCII string. The format is MMDDYYYY. For example, a release date of January 15, 1987 would be 01151987. It is valid after the completion of a controller reset.

Size of Buffer (2 bytes):

These 2 bytes are the amount of on-board buffer RAM expressed in 1K increments. This value is represented as a four-digit hexadecimal number. For example, a 128K RAM buffer would be 0080. This value is valid after the completion of a controller reset.

Current Host Adapter Primary Bus ID (1 byte):

This byte is the current bus ID for the primary SCSI bus. This value is represented as a 1-digit hexadecimal number. This value will default to the bus ID encoded in the on-board switches at the completion of a controller reset. This value will be updated at the completion of an INITIALIZE CONTROLLER command.

Current Host Adapter Secondary Bus ID (1 byte):

This is the current bus ID for the secondary SCSI bus. This value is represented as a 1-digit hexadecimal number. This value will default to the bus ID encoded in the on-board switches at the completion of a controller reset. This value will be updated at the completion of an INITIALIZE CONTROLLER command.

SECTION 3

VMEbus INTERRUPTS

OVERVIEW

At the completion of a command (either successful or terminated with an error or with an exception), the Jaguar notifies the host by generating a Command Complete Interrupt on the VMEbus. The Jaguar can respond to the VMEbus Interrupt Acknowledge Cycle with different Interrupt Vectors based on the cause of the interrupt. (See IOPB Format.) But for those VMEbus systems that allow only one interrupt vector per device, the host can still determine the source of the interrupt by checking the status bits in the Command Response Status Word and the Work Queue Number found in the Command Response Block.

The hardware driving the VMEbus interrupt line is cleared at the completion of the VMEbus Interrupt Acknowledge Cycle. However, a Clear Interrupt operation must also be executed by the host to notify the Jaguar that the interrupt has been properly serviced by the host and that the Jaguar may now post its next interrupt. The host does this by clearing the CRBV/CI bit in the Command Response Block. (See Command Response Status Word (CRSW) of the Command Response Block).

NOTE

Any information that the host needs from the Command Response Block must be accessed before it executes this Clear Interrupt operation.

SECTION 4

I/O PARAMETER BLOCKS AND COMMANDS

OVERVIEW

The MACSI software interface of the Jaguar can handle two distinct types of IOPBs: SCSI IOPBs and Control IOPBs. SCSI IOPBs are commands that are sent to the attached SCSI devices. Control IOPBs are commands for the Jaguar itself (such as an initialization command) that result in local Jaguar action but do not result in any SCSI bus activity.

The following IOPBs are supported by the Jaguar.

SCSI IOPBs

SCSI Pass-Through	(0x20)
SCSI Pass-Through Extended	(0x21)
SCSI Reset	(0x22)

Control IOPBs

Perform Diagnostics	(0x40)
Initialize Controller	(0x41)
Initialize Work Queue	(0x42)
Dump Initialization Parameters	(0x43)
Dump Work Queue Parameters	(0x44)
Flush Work Queue	(0x49)

IOPB FORMAT

Both types of commands require similar information to define their operation. This common information is grouped at the beginning of the IOPB. Command-Specific information is then included at the end of the IOPB, after the common information. Not all commands require all of the common information. Fields not required by a command will be reserved for that command and **must** be set to '0'.

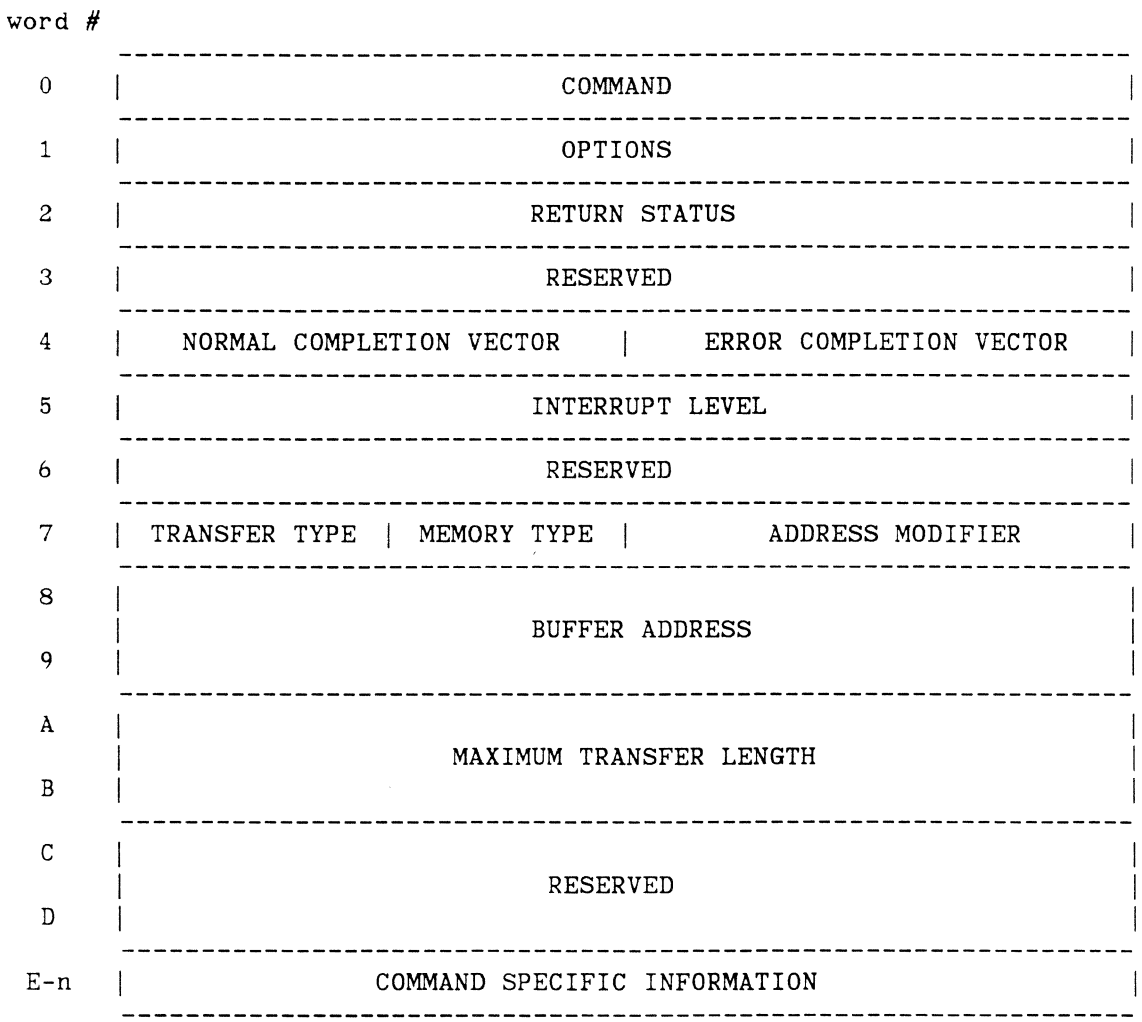


Figure 1 IOPB Format
(n is the length of the IOPB in words)

COMMAND (2 bytes):

These two bytes specify the command to be executed. Section 4 lists all of the commands supported by the Jaguar.

OPTION (2 bytes):

These bytes define the command options that are to be used.

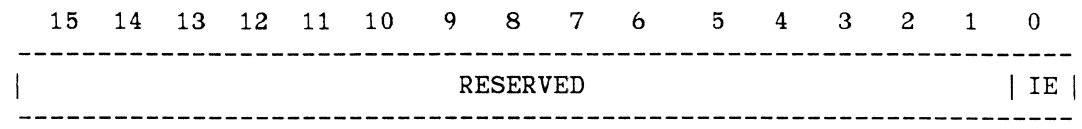


Figure 18. Option

Bit 0 Interrupt Enable (IE):

The Interrupt Enable (IE) bit, when set to '1', enables the Jaguar to interrupt the host upon Command Completion. When set to '0', Command Complete interrupts are disabled.

Bits 1-7 Reserved:

These seven bits are reserved for future options that are **not** command specific. These bits must be set to '0'.

Bits 8-15 Reserved:

This byte is reserved for command specific options. Bits reserved for command options must set to '0' if they are not used.

RETURN STATUS (2 bytes):

These two bytes hold the return status of the command.

NORMAL COMPLETION VECTOR/ERROR COMPLETION VECTOR (2 bytes):

These two bytes specify the interrupt vectors to be used for reporting normal and error command completion.

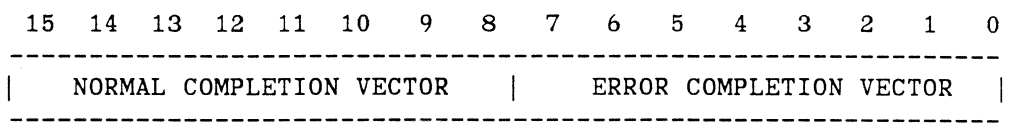


Figure 18. Normal Completion Vector/Error Completion Vector

Bits 0-7 Error Completion Vector:

This byte is the vector used for a Command Complete Interrupt for any error condition.

Bits 8-15 Normal Completion Vector:

This byte is the vector used for a Command Complete Interrupt when no errors occur in the command processing.

INTERRUPT LEVEL (2 bytes):

These two bytes specify the Interrupt Level to be used for both normal and error interrupts.

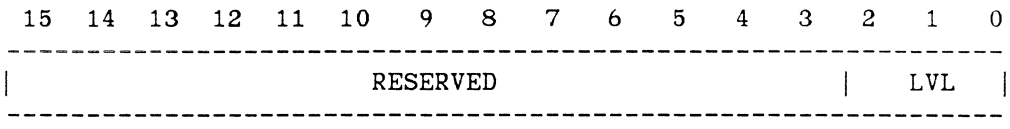


Figure 19. Interrupt Level

Bits 0-2 Interrupt Level (LVL):

These bits set the interrupt level used by the Jaguar to assert a Command Complete Interrupt on the VMEbus. Values of '0' through '7' are allowed. An interrupt level of zero is allowed only when interrupts are disabled (IE = '0' in the Option word).

Bits 3-15 Reserved:

These bits are reserved and must be set to '0' by the host.

MEMORY TYPE/ADDRESS MODIFIER (2 bytes):

These bytes specify the memory type and the address modifier to be used for all VMEbus transfers associated with the command.

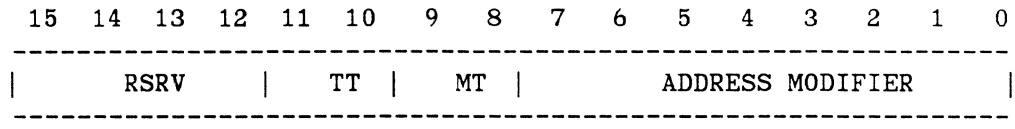


Figure 20. Memory Type/Address Modifier

Bits 0-7 Address Modifier:

This byte is the address modifier used by the Jaguar for all VMEbus data transfers associated with this command. This byte is **not** changed by the Jaguar.

Bits 8-9 Memory Type (MT):

This 2-bit field specifies the width of data transfers.

8-9	FUNCTION
0	Reserved
1	16-bit transfers
2	32-bit transfers
3	Data is contained in the dual ported memory

Figure 21. Memory Type

Bits 10-11 Transfer Type (TT):

This 2-bit field specifies the type of data transfer to be performed. Specific commands may not support all of these modes. All slave devices may not support all of these modes either.

10-11	FUNCTION
0	Normal Mode
1	Block Mode
2	Disable Incrementing Addresses
3	Reserved

Figure 22. Transfer Type

Bits 12-15 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

BUFFER ADDRESS (4 bytes):

These four bytes specify the starting address of the buffer in memory from/to which the Jaguar is to transfer the data.

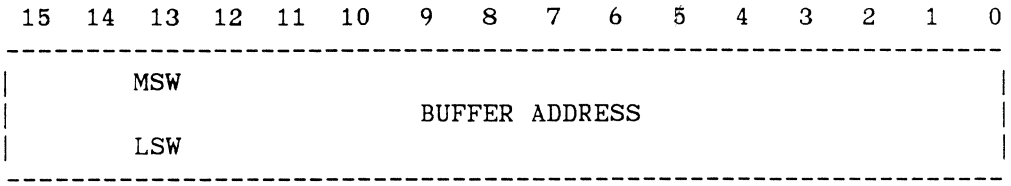


Figure 23. Buffer Address

MAXIMUM TRANSFER LENGTH (4 bytes):

These four bytes specify the maximum amount of data, in bytes, that may be transferred by the command.

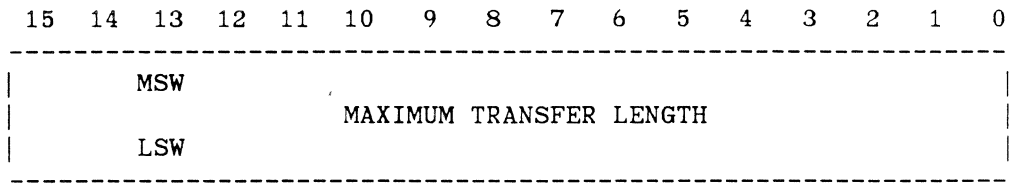


Figure 24. Maximum Transfer Length

SCSI IOPBS

The host uses SCSI IOPBs to send commands to specific SCSI peripherals on either of the SCSI buses attached to the Jaguar. The Jaguar uses these commands to supervise SCSI activity and to transfer data to or from the VMEbus. The Jaguar passes the SCSI command itself across the SCSI bus to the SCSI device for which it is intended without altering or checking it.

The Jaguar supports two types of SCSI Pass-Through command types. The first, SCSI Simple Pass-Through, is used for SCSI commands that are short enough to be included in a **normal** IOPB. SCSI Simple Pass-Through is the only command type normally used.

A second type of Pass-Through, SCSI Extended Pass-Through, is also supported. The SCSI Extended Pass-Through command is provided for handling vendor-unique SCSI commands that are larger than the **normal** IOPB. The IOPB in a SCSI Extended Pass-Through command points to a block of data that contains the actual command to be sent to the SCSI device.

Even though the host can define the maximum IOPB size, defining an unnecessarily large IOPB, just to handle a special vendor-unique SCSI command, is usually not a good choice because it compromises the available work queue space. Thus, it is usually better to define a modest size for normal IOPBs and use the SCSI Extended Pass-Through to handle long SCSI commands.

A third SCSI IOPB type is the SCSI Reset. This IOPB instructs the Jaguar to reset the SCSI bus identified by the command.

SCSI SIMPLE PASS-THROUGH

The SCSI Simple Pass-Through IOPB provides all of the information the Jaguar needs to send a command to a specific SCSI peripheral on either of the SCSI buses. The IOPB includes both the SCSI command and direction of the transfer. Also included are the VMEbus address and type of data buffer for the command. The Jaguar uses this information to execute the command and to interrupt the host when Command Complete status is received from the SCSI device. The Jaguar passes the SCSI command across the SCSI bus to the SCSI device without altering or checking the command.

word #		
0	COMMAND 0x20	
1	OPTIONS	
2	RETURN STATUS	
3	RESERVED	
4	NORMAL COMPLETION VECTOR	ERROR COMPLETION VECTOR
5	INTERRUPT LEVEL	
6	RESERVED	
7	TRANSFER TYPE | MEMORY TYPE	ADDRESS MODIFIER
8	BUFFER ADDRESS	
9		
A	MAXIMUM TRANSFER LENGTH	
B		
C-E	RESERVED	
F	UNIT ADDRESS	
10	SCSI BYTE 0	SCSI BYTE 1
11	SCSI BYTE 2	SCSI BYTE 3
12	SCSI BYTE 4	SCSI BYTE 5
13	SCSI BYTE 6	SCSI BYTE 7
14	SCSI BYTE 8	SCSI BYTE 9
15	SCSI BYTE 10	SCSI BYTE 11

Figure 25. SCSI Simple Pass-Through IOPB

The format for a SCSI Simple Pass-Through IOPB with a 12-byte SCSI command is shown. Longer or shorter SCSI commands are formed by appending the appropriate number of bytes at Word 10 and indicating the correct length in the IOPB length field of the Command Queue Entry.

The following section describes the function of each field in the SCSI Simple Pass-Through IOPB. If the field is used as defined in IOPB Format, no additional description is provided.

Command (2 bytes):

The Command word for SCSI Simple Pass-Through is 0x20h.

Options (2 bytes):

The Options bytes specify the command options that are available.

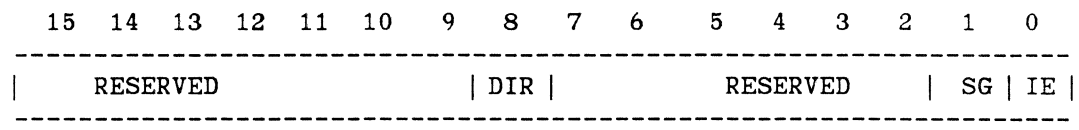


Figure 26. Option

Bit 0 Interrupt Enable (IE):

Bit 1 Scatter/Gather (SG):

When Bit 1 is set to '1', Scatter/Gather is enabled. See Appendix D for a complete description of Scatter/Gather. When Scatter/Gather is enabled, the following fields are defined differently than for non-Scatter/Gather: Memory Type/Address Modifier, Transfer Length, and Buffer Address.

Bits 2-7 Reserved:

These bits are reserved and must be set to '0' by the host.

Bit 8 VME Transfer Direction (DIR):

The VME Transfer Direction (DIR) bit defines the direction of the data transfer over the VMEbus.

Bit 8	VME DIRECTION
0	Data is written to the VMEbus
1	Data is read from the VMEbus

Figure 27. VME Transfer Direction

Bits 9-15 Reserved:

These bits are reserved and must be set to '0' by the host.

Return Status (2 bytes):

These two bytes are the Return Status for the command. The Return Status consists of two fields. The upper byte is the SCSI status as returned from the addressed SCSI device. The lower byte is an error code for controller operations.

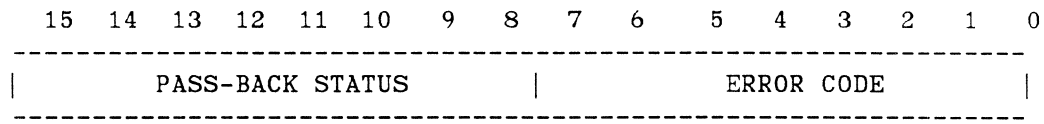


Figure 28. Return Status

Bits 0-7 Error Code:

The Error Code byte describes the status of the controller at the end of the command response.

Bits 8-15 Pass-Back Status:

The Pass-Back Status byte is the status byte returned by the SCSI target device. This byte is not changed by the Jaguar.

Address Modifier/Memory Type/Transfer Type (2 bytes):

These two bytes specify the memory type and address modifier to be used for any VMEbus transfers associated with the command. When scatter gather is enabled, this field is set for the Scatter/Gather List Memory Type/Address Modifier.

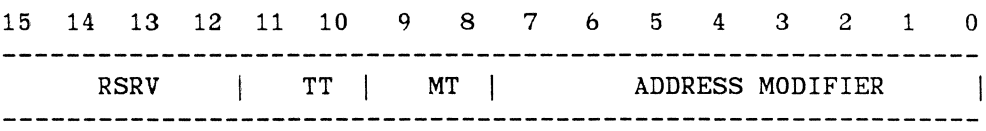


Figure 29. Address Modifier/Memory Type/Transfer Type

Bits 0-7 Address Modifier:

This byte is the address modifier used for VMEbus data transfers associated with the command. This byte is not changed by the Jaguar.

Bits 8-9 Memory Type (MT):

This 2-bit field specifies the width of the data transfer.

8-9	FUNCTION
0	Reserved
1	16-bit transfers
2	32-bit transfers
3	Reserved

Figure 30. Memory Type

Bits 10-11 Transfer Type (TT):

10-11	FUNCTION
0	Normal Mode
1	Block Mode
2	Disable Incrementing Addresses
3	Reserved

Figure 31. Transfer Type

Bits 12-15 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

Buffer Address (4 bytes):

When scatter gather is enabled, this field is the address of the Scatter/Gather List.

Maximum Transfer Length (4 bytes):

The Transfer Length specifies the maximum amount of data, in bytes, the device may transfer with this command. If no data is to be transferred, a Transfer Length of zero should be specified. When Scatter/Gather is enabled, this field comprises the number of scatter gather elements.

Unit Address (2 bytes):

This Unit Address specifies the SCSI bus and the address of the target SCSI device to be used for the SCSI command.

15 14 13 12 11 10 9 8	7	6 5 4	3 2 1 0
EXTENDED ADDRESS	EXT BUS	LUN	SCSI ID

Figure 32. Unit Address

Bits 0-2 SCSI Device ID (SCSI ID):

These three bits are the SCSI Bus ID (SCSI ID) of the specified device.

Bits 3-5 Logical Unit Number (LUN):

These bits describe the SCSI Logical Unit Number (LUN) of the specified device.

Bit 6 SCSI Bus Selection (BUS):

The SCSI Bus Selection (BUS) bit selects which of the two SCSI buses the Jaguar uses when executing the command. When the BUS bit is set to '0', the Jaguar executes the command over the primary SCSI bus. When set to '1', it uses the secondary SCSI bus.

Bit 7 Extended Addressing Enable (EXT):

The Extended Addressing Enable (EXT) bit is set to '1' to enable the use of Extended SCSI Addressing. When Extended Addressing is enabled, bits 8 through 15 specify the Extended Address.

Bits 8-15 Extended Address:

These bits describe the address when Extended SCSI Addressing is used.

SCSI Command Bytes:

The SCSI Command Bytes specify the bytes that the Jaguar passes unchanged across the SCSI bus to the selected SCSI device. The length of this field is determined by the IOPB Length byte specified in the CQE. (See IOPB Length). It is also limited by the maximum IOPB length specified by the host during initialization. (See Initialize Controller Command, Controller Initialization Block).

SCSI EXTENDED PASS-THROUGH

The SCSI Extended Pass-Through command accommodates vendor-unique SCSI commands that are longer than normal IOPBs. The IOPB in a SCSI Extended Pass-Through command points to a block of data that contains the actual command to be sent to the SCSI device. The host must preserve this SCSI Command block until it receives a "Command Complete" for the IOPB.

The host indirectly defines the maximum IOPB size by defining the size of the Command Response Block (which must be large enough to hold any returned IOPB). Nevertheless, defining an unnecessarily large IOPB, just to handle a special vendor-unique SCSI command, usually is not a good choice because it decreases the available work queue Space. It is usually better to define a modest size for normal IOPBs and use the SCSI Extended Pass-Through to handle long SCSI commands.

See Controller Initialization Block, Command Response Block Offset for more details of defining the maximum IOPB length.

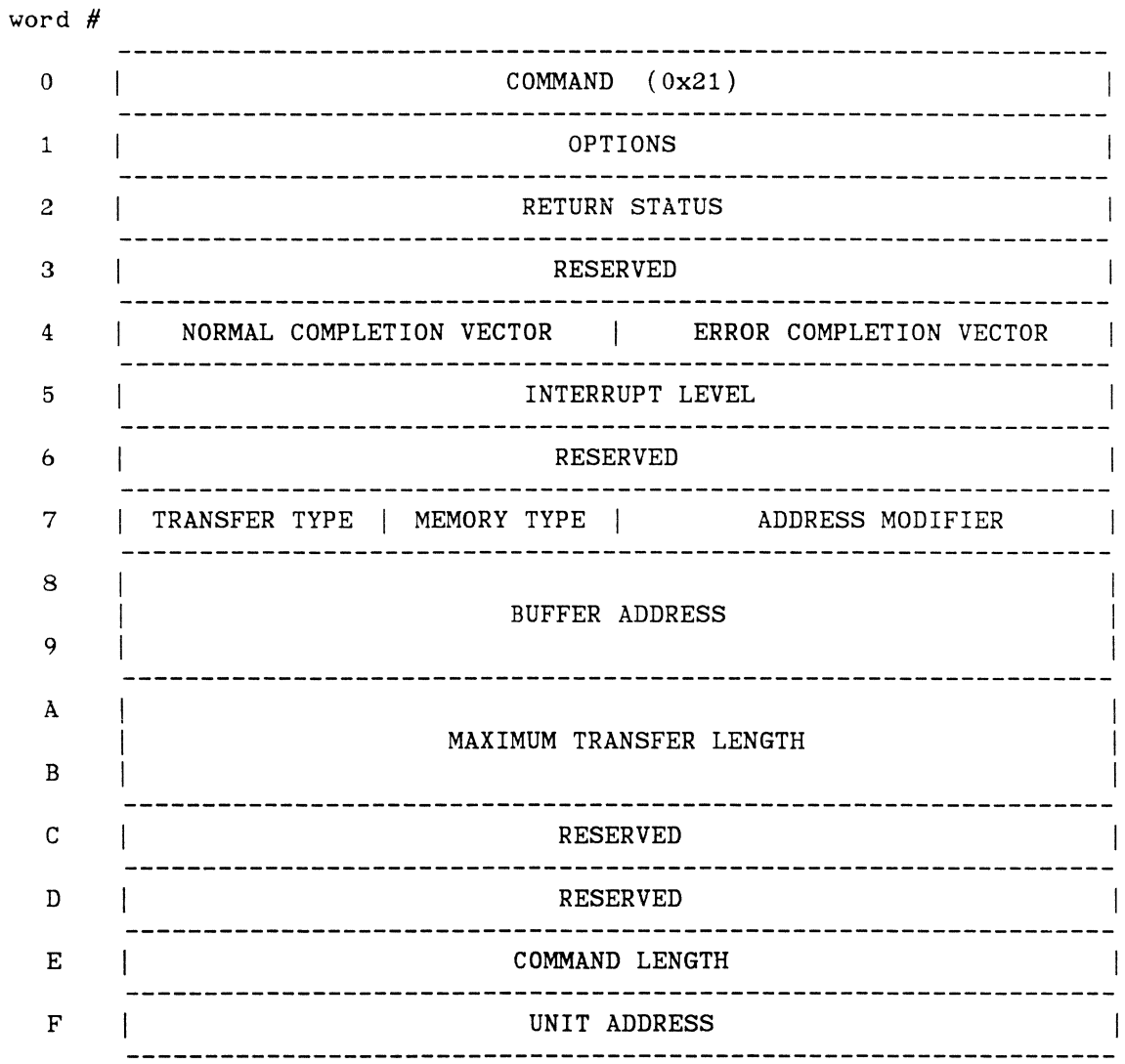


Figure 33. SCSI Extended Pass-Through IOPB

The following section describes the function of each field in the SCSI Extended Pass-Through IOPB. If the field is used as defined in IOPB Format, no additional description is provided.

Command (2 bytes):

The Command word for SCSI Extended Pass-Through is 0x21h.

Options (2 bytes):

These two bytes specify the command options available.

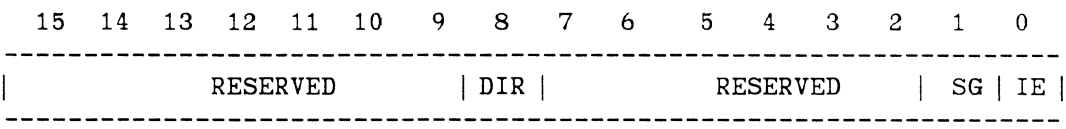


Figure 34. Options

Bit 0 Interrupt Enable (IE):

Bit 1 Scatter/Gather (SG):

When bit 1 is set to '1', Scatter/Gather is enabled. See Appendix D for a complete description of Scatter/Gather. When Scatter/Gather is enabled, the following fields are defined differently than for non-Scatter/Gather: Memory Type/Address Modifier, Transfer Length, and Buffer Address.

Bits 2-7 Reserved:

These bits are reserved and must be set to '0' by the host.

Bit 8 VME Transfer Direction (DIR):

The VME Transfer Direction (DIR) bit defines the direction of the data transfer over the VMEbus.

Bit 8	VME DIRECTION
0	Data is written to the VMEbus
1	Data is read from the VMEbus

Figure 35. VME Transfer Direction

Bits 9-15 Reserved:

These bits are reserved and must be set to '0' by the host.

Return Status (2 bytes):

These bytes are the Return Status for the command. The Return Status consists of two fields. The upper byte is the SCSI status as returned from the addressed SCSI device. The lower byte is an error code for controller operations.

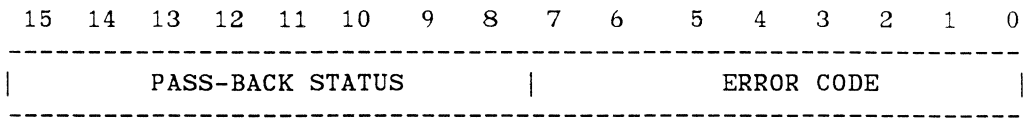


Figure 36. Return Status

Bits 0-7 Error Code:

The Error Code byte describes the status of the controller at the end of the command response.

Bits 8-15 Pass-Back Status:

The Pass-Back Status byte is the status byte returned by the SCSI target device. This byte is not changed by the Jaguar.

Address Modifier/Memory Type/Transfer Type (2 bytes):

These 2 bytes specify the address modifier, memory type and transfer type to be used for any VME transfers associated with the command.

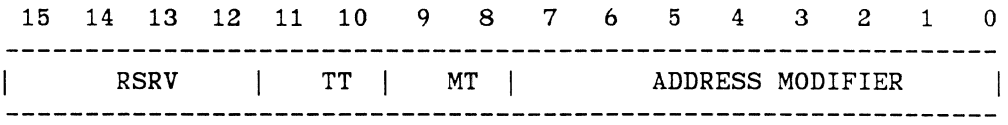


Figure 37. Address Modifier/Memory Type/Transfer Type

Bits 0-7 Address Modifier:

This byte is the address modifier used for VMEbus data transfers associated with this command. This byte is not changed by the Jaguar.

Bits 8-9 Memory Type (MT):

This 2-bit field specifies the width of the data transfer.

8-9	FUNCTION
0	Reserved
1	16-bit transfers
2	32-bit transfers
3	Reserved

Figure 38. Memory Type

Bits 10-11 Transfer Type (TT):

10-11	FUNCTION
0	Normal Mode
1	Block Mode
2	Disable Incrementing Addresses
3	Reserved

Figure 39. Transfer Type

Bits 12-15 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

Buffer Address (4 bytes):

The Buffer Address contains the offset in the dual ported memory of the Command Block to be sent to the attached SCSI device.

Maximum Transfer Length (4 bytes):

The Transfer Length specifies the maximum amount of data, in bytes, the command will transfer. If no data is to be transferred, a length of zero should be specified.

Command Length (2 bytes):

The Command Length specifies the length, in bytes, of the SCSI command to which this IOPB points.

Unit Address (2 bytes):

The Unit Address specifies the SCSI bus and the address of the target SCSI device to be used for the SCSI command.

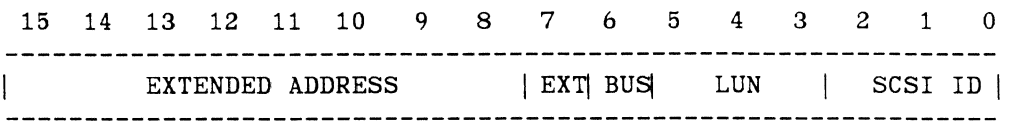


Figure 40. Unit Address

Bits 0-2 SCSI Device ID (SCSI ID):

These 3 bits are the SCSI Bus ID (SCSI ID) of the specified device.

Bits 3-5 Logical Unit Number (LUN):

These bits describe the SCSI Logical Unit Number (LUN) of the specified device.

Bit 6 SCSI Bus Selection (BUS):

The SCSI Bus Selection (BUS) bit selects which of the two SCSI buses the Jaguar uses when executing the command. When the BUS bit is set to '0', the Jaguar executes the command over the primary SCSI bus. When set to '1', it uses the secondary SCSI bus.

Bit 7 Extended Addressing Enable (EXT):

The Extended Addressing Enable (EXT) bit is set to '1' to enable the use of Extended SCSI Addressing. When Extended Addressing is enabled, bits 0 through 7 specify the Extended Address.

Bits 8-15 Extended Address:

These bits describe the address when Extended SCSI Addressing is used.

SCSI COMMAND BLOCK

The Buffer Address pointer of the SCSI Extended Pass-Through IOPB points to a SCSI Extended Pass-Through Command Block. The host must assemble this Command Block in the dual-ported memory of the Jaguar exactly as it wants it passed to the SCSI device.

word #		
0	BUFFER ADDRESS	
1		
2	MAXIMUM TRANSFER LENGTH	
3		
4	SCSI BYTE 0	SCSI BYTE 1
5	SCSI BYTE 2	SCSI BYTE 3
6	SCSI BYTE 4	SCSI BYTE 5
7	SCSI BYTE 6	SCSI BYTE 7
8	SCSI BYTE 8	SCSI BYTE 9
N	SCSI BYTE ((N-4)*2)	SCSI BYTE ((N-4)*2) + 1

Figure 41. SCSI Extended Pass-Through Command Block

SCSI RESET IOPB

The SCSI Reset IOPB instructs the Jaguar to reset the SCSI bus identified by the command. It terminates all pending commands on the SCSI bus. A Command Complete with Error will be issued for each command terminated as a result of the SCSI Reset command.

Normally, this command is used only in an to attempt to recover from an unusual error condition.

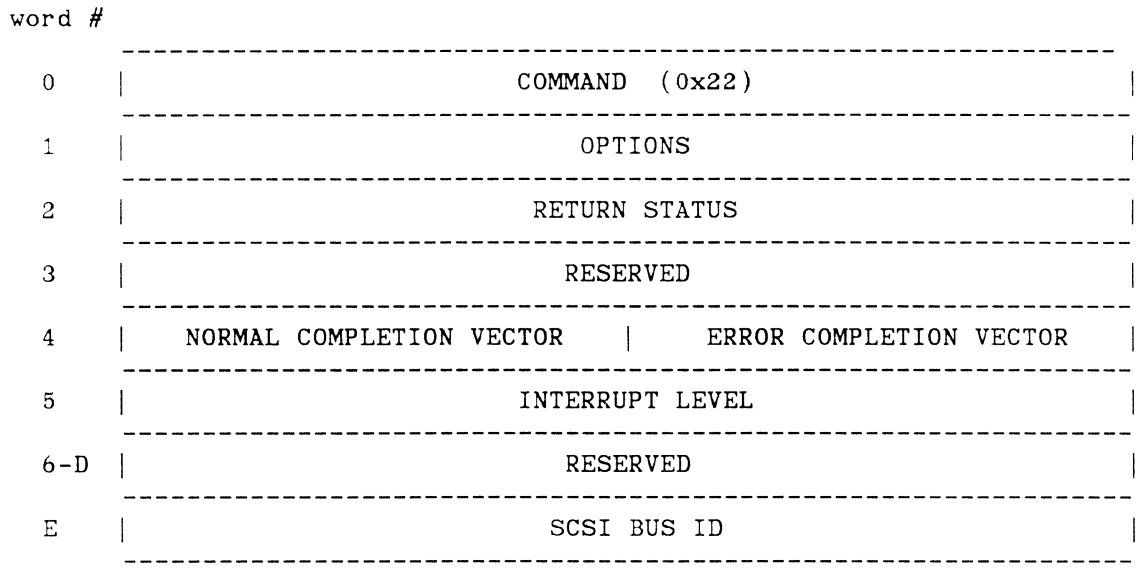


Figure 42. SCSI Reset IOPB

The following section describes the function of each field in the SCSI Reset IOPB. If the field is used as defined in IOPB Format, no additional description is provided.

Command (2 bytes):

The Command word for SCSI Reset is 0x22h.

Option (2 bytes):

Return Status (2 bytes):

Normal Completion Vector/Error Completion Vector (2 bytes):

Interrupt Level (2 bytes):

SCSI Bus ID (2 bytes):

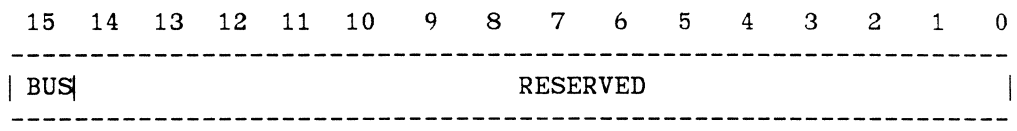


Figure 43. SCSI Bus ID

Bits 0-14 Reserved:

These bits are reserved and must be set to '0'.

Bit 15 SCSI Bus Selection (BUS):

The SCSI Bus Selection (BUS) bit selects which of the two SCSI buses the Jaguar uses when executing the command. When the BUS bit is set to '0', the Jaguar executes the command over the primary SCSI bus. When set to '1', it uses the secondary SCSI bus.

CONTROL IOPBs

A Control IOPB (CIOPB) is a command to the Jaguar that does not result in any SCSI bus activity. The Control IOPBs that the Jaguar recognizes are listed below:

Perform Diagnostics	(0x40)
Initialize Controller	(0x41)
Initialize Work Queue	(0x42)
Dump Initialization Parameters	(0x43)
Dump Work Queue Parameters	(0x44)
Flush Work Queue	(0x49)

PERFORM DIAGNOSTICS COMMAND

The Perform Diagnostics command causes the Jaguar to perform a set of self-diagnostic tests that are more extensive than those performed during the power-up self test. These self-diagnostic tests include an extensive RAM test (scratchpad, buffer, and event RAM). All of the tests are performed, and then the status of each test is reported back in the

Command Response Block. Due to the nature of these tests, the Perform Diagnostics command cannot be executed while the Jaguar is operating. The Jaguar returns an error if this command is issued while ANY other command is queued.

Since it takes several minutes for the Jaguar to complete such a thorough self-diagnostic routine (and due to the relative completeness of the power-up self tests), this command probably should **not** be used as part of the normal initialization routine in a system driver.

The Perform Diagnostics command **must** be issued through the MCE.

The format of the CIOPB for the Perform Diagnostics command is as follows:

word #	
0	COMMAND (0x40)
1	RESERVED
2	RESERVED
3-D	RESERVED
E	ROM TEST RESULT
F	SCRATCHPAD RAM TEST RESULT
10	BUFFER RAM TEST RESULT
11	EVENT RAM TEST RESULT
12	SCSI PRIMARY PORT REGISTER TEST
13	SCSI SECONDARY PORT REGISTER TEST

Figure 44. Perform Diagnostics Command Format

In all cases, a test result of 0xFFFF indicates a successful test. Any other value indicates an error code.

Command (2 bytes):

The command code is 0x40.

ROM Test Result (2 bytes):

These bytes return the status of the ROM Test.

Scratchpad RAM Test Result (2 bytes):

These bytes return the status of the Scratchpad RAM Test.

Buffer RAM Test Result (2 bytes):

These bytes return the status of the Buffer RAM Test.

Event RAM Test Result (2 bytes):

These bytes return the status of the Event RAM Test.

SCSI Primary Port Register Test (2 bytes):

These bytes return the status of the SCSI Primary Port Register Test.

SCSI Secondary Port Register Test (2 bytes):

These bytes return the status of the SCSI Secondary Port Register Test.

INITIALIZE CONTROLLER COMMAND

The Initialize Controller command configures the Jaguar for use in a particular system. The host must issue the Initialize Controller command before the Jaguar can engage in any activity on the SCSI bus. Since Command Queues are not initialized when the Initialize Controller command is issued, the host must use the Master Command Entry to issue the Initialize Controller command. The Master Command Entry (MCE) must point to Work Queue 0 (see Master Command Entry). The format of the CIOPB for the Initialize Controller command is:

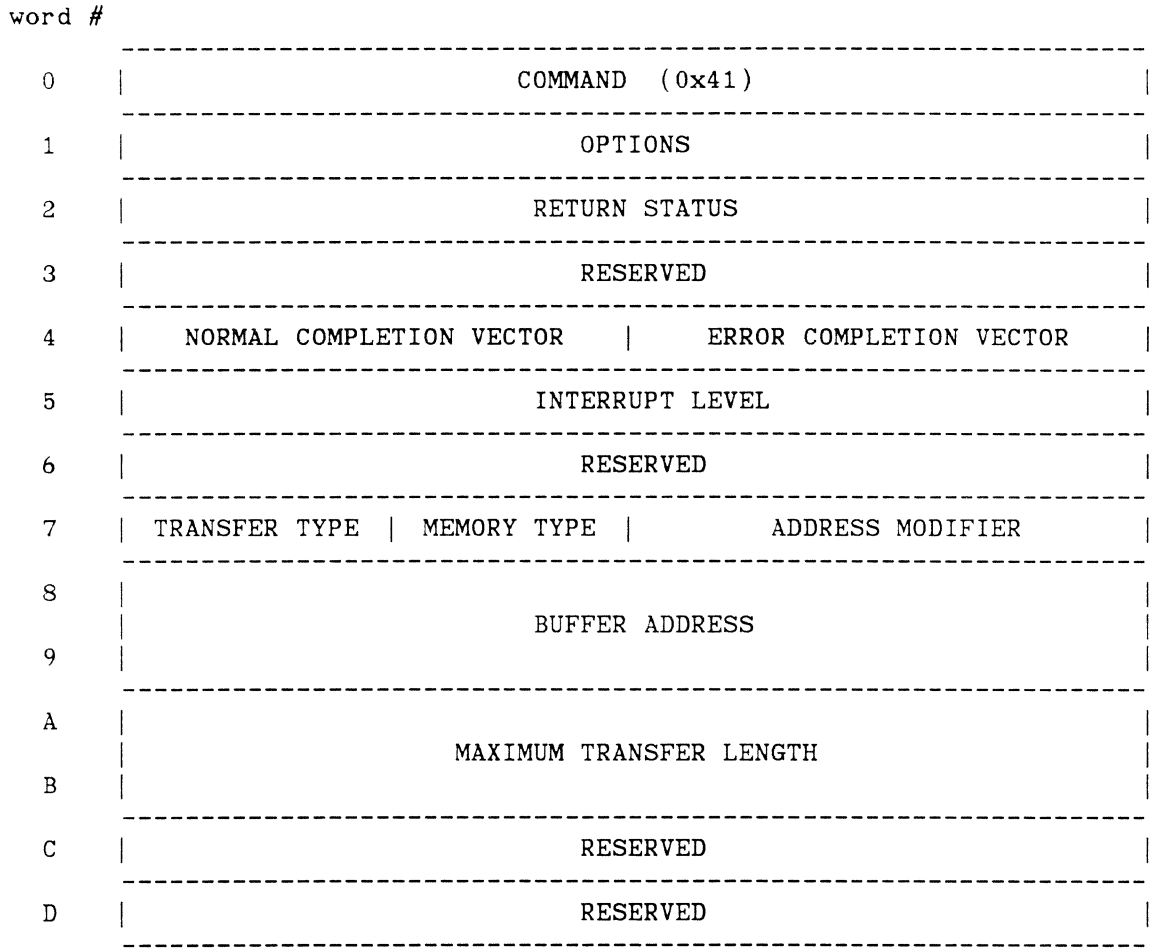


Figure 45. Initialize Controller Command Format

The following section describes the function of each field in the Initialize Controller IOPB. If the field is used as defined in IOPB Format, no additional description is provided.

Command (2 bytes):

The command code for the Initialize Controller Command is 0x41.

Option (2 bytes):

Return Status (2 bytes):

Normal Completion Vector/Error Completion Vector (2 bytes):

Interrupt Level (2 bytes):

Address Modifier/Memory Type/Transfer Type (2 bytes):

These bytes specify the address modifier, memory type and transfer type to be used for the VMEbus transfers associated with the Initialize Controller command.

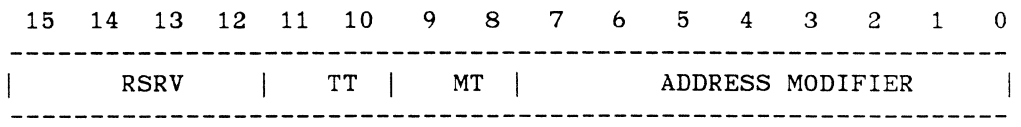


Figure 46. Address Modifier/Memory Type/Transfer Type

Bits 0-7 Address Modifier:

This byte must be set to 0x00 in the Initialize Controller Command.

Bits 8-9 Memory Type (MT):

The data for this command must be contained in the dual ported memory, so bits 8 and 9 must both set to be '1'.

8-9	FUNCTION
0	Reserved
1	Reserved
2	Reserved
3	Data is contained in the dual ported memory

Figure 47. Memory Type

Bits 10-11 Transfer Type (TT):

This 2-bit field must be set to '0'.

Bits 12-15 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

Buffer Address (4 bytes):

These bytes specify the offset of the Controller Initialization Block from the start of the dual ported memory.

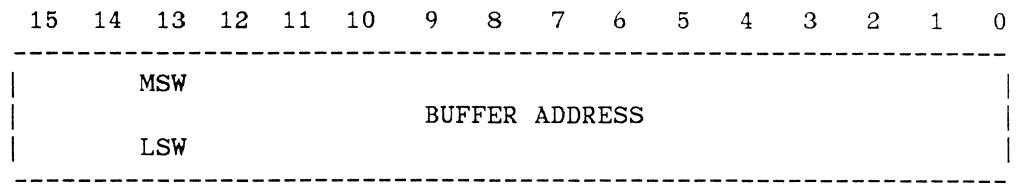


Figure 48. Buffer Address

Maximum Transfer Length (4 bytes):

CONTROLLER INITIALIZATION BLOCK (CIB)

The Buffer Address of the Initialize Controller IOPB points to a list of initialization parameters called the Controller Initialization Block (CIB). The host must assemble the Controller Initialization Block in the Host Usable Space (HUS) before an Initialize Controller command may be issued. The host cannot modify the CIB until it receives a command complete interrupt for the Initialize Controller command.

Words 7-8, 9-0xA, and 0xB-0xC have been added to the Controller Initialization Block. A value of '0' in any of these words provides operation identical to previous revisions of the firmware. Therefore, no change is required for existing software unless it is desired to use these features.

The format of the CIB is as follows:

word #	
0	NUMBER OF COMMAND QUEUE ENTRIES
1	DMA BURST COUNT
2	CONTROLLER NORMAL COMPLETION VECTOR
3	CONTROLLER ERROR COMPLETION VECTOR
4	PRIMARY SCSI BUS ID
5	SECONDARY SCSI BUS ID
6	COMMAND RESPONSE BLOCK OFFSET
7-8	SCSI SELECTION TIME OUT
9-0xA	SCSI RE-SELECTION TIME OUT
0xB-0xC	VMEBUS TIME OUT
0xD-0xF	RESERVED

Figure 49. Controller Initialization Block

The following is a description of each field in the Controller Initialization Block.

Number of Command Queue Slots (2 bytes):

The number of slots in each Command Queue. The maximum number of slots in any one Command Queue is 40.

DMA Burst Count (2 bytes):

The DMA Burst Count is the number of VMEbus DMA transfers the Jaguar will perform in a single burst before releasing the bus and re-requesting it. The Jaguar, with the BUSpacket Interface, has a maximum burst length of 256 16-bit transfers or 128 32-bit transfers. Setting the DMA Burst Count to '0' causes the Jaguar to use the maximum burst count. The burst count is the number of bytes per burst or, in other words, bytes per VMEbus DMA transfers.

Controller Normal Completion Vector (2 bytes):

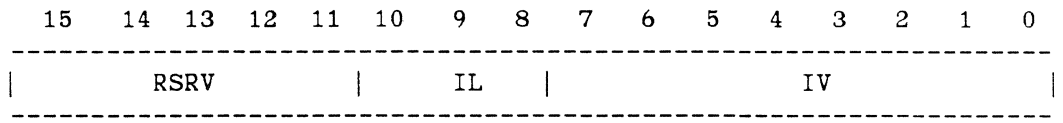


Figure 50. Controller Normal Completion Vector

Bits 0-7 Interrupt Vector (IV):

This byte is the Interrupt Vector used by the Jaguar when reporting the normal completion of any Initialize Controller command. The host sets this byte and it is not modified by the Jaguar.

Bits 8-10 Interrupt Level (IL):

These bits set the Interrupt Level used by the Jaguar when reporting the normal completion of any Initialize Controller command. The host sets these bits and the Jaguar does not modify them.

Bits 11-15 Reserved (RSRV):

Bits 11 through 15 are reserved and should be set to '0' by the host.

Controller Error Completion Vector (2 bytes):

The Controller Error Completion Vector is used by the Jaguar when reporting the error completion of the following commands: Start Queued Mode, Flush All Queues and Report, and Flush All Queues.

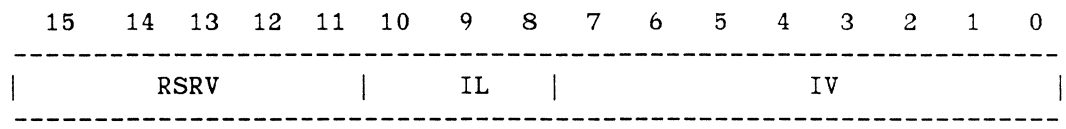


Figure 51. Controller Error Completion Vector

Bits 0-7 Interrupt Vector (IV):

This byte is the Interrupt Vector used by the Jaguar when reporting the Error Completion of any Initialize Controller command. The host sets this byte and it is not modified by the Jaguar.

Bits 8-10 Interrupt Level (IL):

These bits set the Interrupt Level used by the Jaguar when reporting the Error Completion of any Initialize Controller command. The host sets these bits and the Jaguar does not modify them.

Bits 11-15 Reserved (RSRV):

Bits 11 through 15 are reserved and should be set to '0' by the host.

Primary SCSI Bus ID (2 bytes):

The Primary SCSI Bus ID specifies the ID the Jaguar uses for the SCSI bus address on its primary SCSI port. The Jaguar can either use its default ID or it may use the value given in bits 0 through 2.

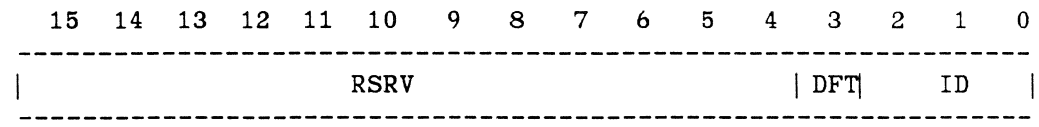


Figure 52. Primary SCSI Bus ID

Bits 0-2 Primary SCSI Bus ID (ID):

The host uses these bits to specify the SCSI ID the Jaguar is to use for the primary Port when the DFT bit is '0'. This field may have any value from '0' to '7'.

Bit 3 Default (DFT):

Setting the Default bit to '1' enables the Jaguar to use the default ID specified by the on board DIP switches. Setting the Default bit to '0' causes the Jaguar to use the ID specified in the ID field (bits 0-2) of this word.

Bits 4-15 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

Secondary SCSI Bus ID (2 bytes):

The Secondary SCSI Bus ID specifies the ID the Jaguar uses for the SCSI bus address on its secondary SCSI port. The Jaguar can either use its default ID or it may use the value given in bits 0 through 2.

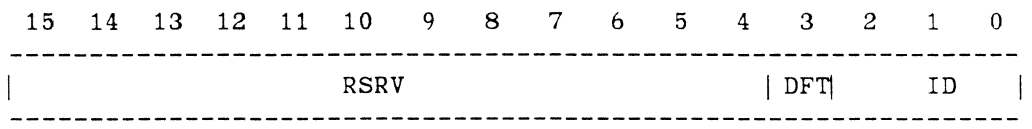


Figure 53. Secondary SCSI Bus ID

Bits 0-2 Secondary SCSI Bus ID (ID):

The host uses these 3 bits to specify the SCSI ID the Jaguar is to use for the secondary Port when the DFT bit is '0'. This field may have any value from '0' to '7'.

Bit 3 Default (DFT):

Setting the Default bit to '1' enables the Jaguar to use the default ID specified by the on board DIP switches. Setting the Default bit to a '0' causes the Jaguar to use the ID specified in the ID field (bits 0-2) of this word.

Bits 4-15 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

Command Response Block Offset:

The Command Response Block Offset word specifies the starting address of the Command Response Block. By setting the Command Response Block Offset, the host is also specifying the length of the largest IOPB that can be transferred to the Jaguar. The largest IOPB is equal to the offset of the Controller Specific Space (0x788) minus the Command Response Block Offset, minus 12 bytes. If the Command Response Block Offset is 0x73C, for example, the largest IOPB cannot exceed 64 bytes (0x788 - 0x73C - 0xC).

The Command Response Block Offset must allow for a Command Response Block of at least 18 bytes so that there will always be enough room in the Command Response Block to include the status bytes of the returned IOPB. Attempting to use a Command Response Block Offset that would result in a Command Response Block of less than 18 bytes will result in the Initialize Controller Command completing with an error.

SCSI Selection Time Out:

This long word field specifies the length of time the Jaguar will wait for a device to respond to selection. A value of '0' specifies an infinite time out. Any other value is measured in increments of 1 millisecond.

SCSI Re-Selection Time Out:

This time out specifies a watchdog time out value for devices to re-select after disconnecting. A value of '0' will specify an infinite time out. Any other value is measured in increments of 32 milliseconds.

VMEbus Time Out:

This long word field specifies the length of time the Jaguar will wait for a VME transfer to complete. A value of '0' specifies a time out of 100 milliseconds. Any other value is measured in increments of 32 milliseconds.

INITIALIZE WORK QUEUE COMMAND

The Initialize Work Queue command configures an individual work queue. The Jaguar can have up to 14 work queues in addition to Work Queue 0. Each work queue must be initialized with a separate Initialize Work Queue command.

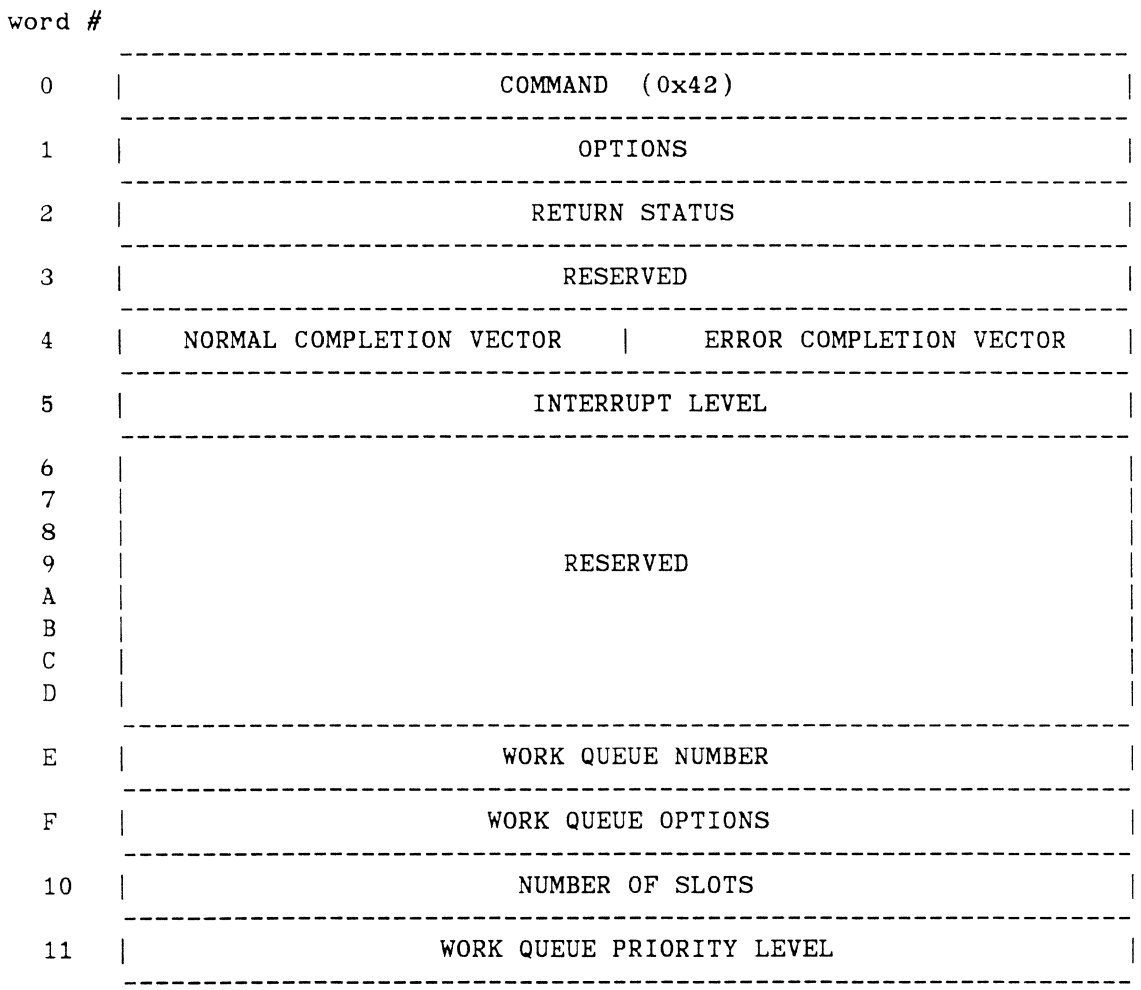


Figure 54. Initialize Work Queue Command Format

The host specifies the following information in the Initialize Work Queue command:

Command (2 bytes):

The command code for the Initialize Work Queue command is 0x42.

Options (2 bytes):

Work Queue Number (2 bytes):

This number identifies which work queue to initialize. After the Initialize Work Queue command has completed, this number is used to indicate into which work queue to place a command block and to determine which work queue has completed a command. Therefore, each work queue must be assigned a unique number. This value must be from 1 to 14.

Work Queue Options (2 bytes):

The host uses the Work Queue Option word to select certain Work Queue options. The host can specify whether the work queue should be flushed when an error condition is encountered or if the work queue should be processed as normal after an error.

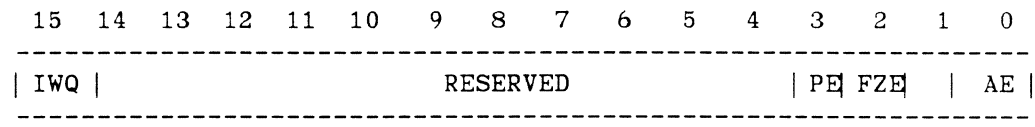


Figure 55. Work Queue Options

Bit 0 Abort Enable (AE):

By setting the Abort Enable (AE) bit to '1', the host enables the Jaguar to abort all IOPBs in the work queue, and all IOPBs in the CQE destined for the work queue, when an IOPB from this queue completes with an error.

By setting the Abort Enable (AE) bit to '0', the host disables the aborting of remaining queue entries when one command terminates with an error. (See Queue Entry Control Register, Abort Acknowledge bit).

Bits 1 and 4-14 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

Bit 2 Freeze Work (FZE):

The Freeze Work bit (FZE) is set during the Work Queue Init command. This attribute will be in effect for that queue only. All commands that do not return a good status will freeze the queue. When the host sees a command return from a work queue that has Freeze on Error enabled with a SCSI device error, the host must unfreeze (thaw) the work queue after taking the error handling steps needed for that particular error.

The frozen work queue is unfrozen by selecting that work queue number in the Thaw Queue Register and then setting Bit 0 of that register. The Jaguar will clear the register to acknowledge the thawing of the work queue. The Thaw Work Queue Status Register is located in the fourth word of the Master Control/Status Block. (See Appendix C).

Bit 3 Parity Enable (PE):

The Parity Enable bit enables SCSI busy parity checking for commands issued from the work queue.

Bit 15 Initialize Work Queue (IWQ):

The Initialize Work Queue (IWQ) bit causes the Jaguar to initialize the work queue even if it has been previously initialized. If commands are pending when the Jaguar attempts to execute an Initialize Work Queue command, the Initialize Work Queue IOPB will not be executed and the IOPB will return with an error status.

Number of Slots (2 bytes):

The Number of Slots word determines the number of slots in the work queue.

Work Queue Priority Level (2 bytes):

The Work Queue Priority Level sets the relative priority of each work queue in relation to the other work queues. The Work Queue Priority Level must be from set from '1' to '14' (with '1' being the highest priority). Work queues given the same Work Queue Priority Level are considered to have the same priority and are serviced in a round robin fashion.

DUMP INITIALIZATION PARAMETERS

The Dump Initialization Parameters command causes the Jaguar to report its current initialization/setup information to the host. This command is intended to be used primarily for diagnostic purposes. The format of the CIOPB for the Dump Initialization Parameters command is shown below:

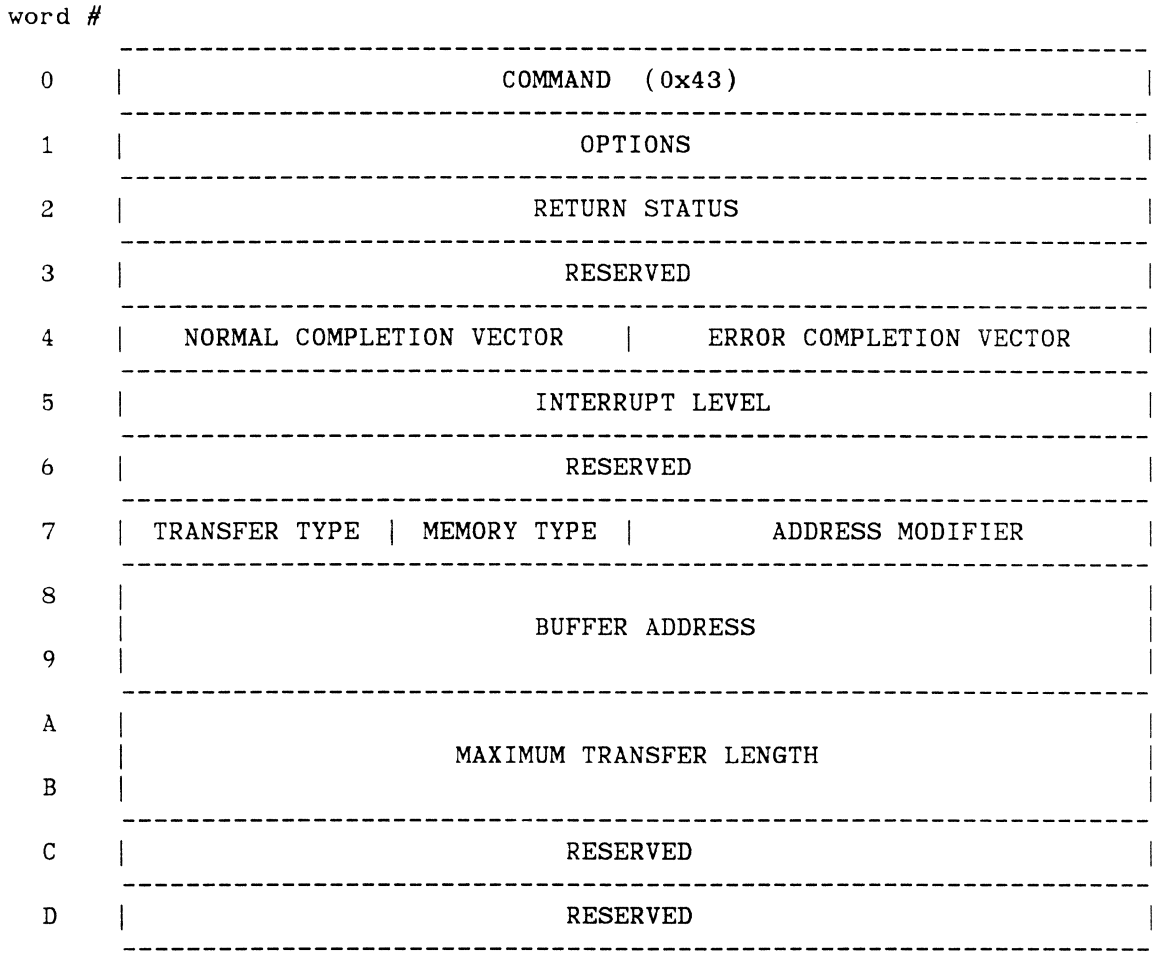


Figure 56. Dump Initialization Parameters

The following section describes the function of each field in the Dump Initialization Parameters IOPB. If the field is used as defined in IOPB Format, no additional description is provided.

Command (2 bytes):

The command code for the Dump Initialization Parameters command is 0x43.

Option (2 bytes):

Return Status (2 bytes):

Normal Completion Vector/Error Completion Vector (2 bytes):

Interrupt Level (2 bytes):

Address Modifier/Memory Type/Transfer Type (2 bytes):

This specifies the memory type and address modifier to be used for any VMEbus transfers associated with the Dump Initialization Parameters command.

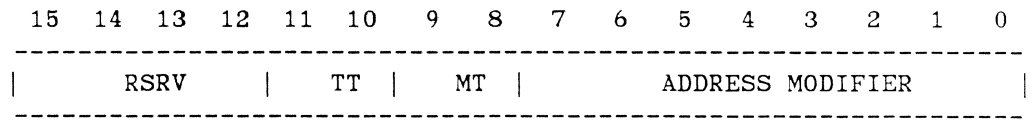


Figure 57. Address Modifier/Memory Type/Transfer Type

Bits 0-7 Address Modifier:

This byte must be set to '0' for the Dump Initialization Parameters command.

Bits 8-9 Memory Type (MT):

The data for this command must be contained in the dual ported memory, so both bits 8 and 9 must be set to '1'.

8-9	FUNCTION
0	Reserved
1	Reserved
2	Reserved
3	Data is contained in the dual ported memory

Figure 58. Memory Type

Bits 10-11 Transfer Type (TT):

These bits must be set to '0'.

Bits 12-15 Reserved (RSRV):

These bits are reserved and must be set to '0' by the host.

Buffer Address (4 bytes):

These bytes specify the offset of the Dump Initialization Parameters Block from the start of the dual ported memory.

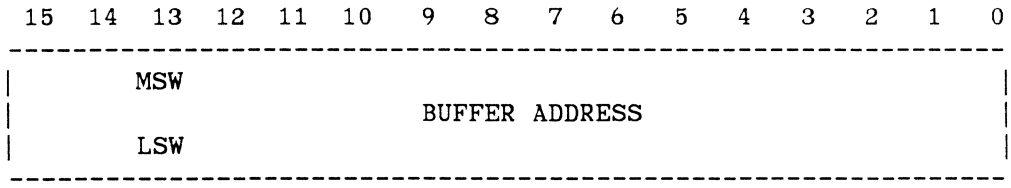


Figure 59. Buffer Address

Transfer Length (4 bytes):

DUMP INITIALIZATION PARAMETER BLOCK

The host must reserve space in the Host Usable Space (HUS) for the return of the list of initialization parameters. This list is pointed to by the Buffer Address pointer of the Dump Initialization Parameters Block CIOPB (see Initialize Controller command for the definition of the values returned by the Dump Initialization Parameters Block command). The following information is provided in the Initialization Parameters Block:

word #	
0	NUMBER OF COMMAND QUEUE SLOTS
1	DMA BURST COUNT
2	CONTROLLER NORMAL COMPLETION VECTOR
3	CONTROLLER ERROR COMPLETION VECTOR
4	PRIMARY SCSI BUS ID
5	SECONDARY SCSI BUS ID
6	COMMAND RESPONSE BLOCK OFFSET
7-F	RESERVED (18 bytes)

Figure 60. Dump Initialization Parameters Block

DUMP WORK QUEUE PARAMETERS

The Dump Work Queue Parameters command causes the Jaguar to report the current parameters of an individual work queue to the host. The format of this IOPB is the same as that of the Initialize Work Queue command.

The host provides the work queue number. If the parameters for a work queue that has not been initialized are requested, the command will complete with an error and an illegal parameter status. The format of the CIOPB for the Dump Work Queue Parameters command is shown on the following page:

word #		
0	COMMAND (0x44)	
1	OPTIONS	
2	RETURN STATUS	
3	RESERVED	
4	NORMAL COMPLETION VECTOR	ERROR COMPLETION VECTOR
5	INTERRUPT LEVEL	
6	RESERVED	
7	RESERVED	
8	RESERVED	
9	RESERVED	
A	RESERVED	
B	RESERVED	
C	RESERVED	
D	RESERVED	
E	WORK QUEUE NUMBER	
F	WORK QUEUE OPTIONS	
10	NUMBER OF SLOTS	
11	WORK QUEUE PRIORITY LEVEL	

Figure 61. Dump Work Queue Parameters

The following section describes the function of each field in the Dump Work Queue Parameters IOPB. If the field is used as defined in IOPB Format, no additional description is provided.

The format of the parameters returned in response to the Dump Work Queue Parameters command is the same as that returned in response to the Initialize Work Queue command.

Command (2 bytes):

The command code for the Dump Work Queue command is 0x44.

Options (2 bytes):

Work Queue Number (2 bytes):

This number identifies the work queue for which parameters are being dumped. If the work queue specified has not been initialized, the command will complete with an error and an illegal parameter status.

Work Queue Options (2 bytes):

Number of Slots (2 bytes):

Work Queue Priority Level (2 bytes):

FLUSH WORK QUEUE COMMAND

The Flush Work Queue command flushes all commands that have been placed in the work queue as well as any commands in the Command Queue destined for the work queue. (This is different from the Flush Queue bits in the Master Control Register. This command flushes only the specified work queue; the Flush Queue bits in the MCR flush all the queues.) This command specifies the work queue number and has, as an option, the ability to report completion of each entry in the queue.

At the completion of the Flush Work Queue command, the number of entries flushed from the queue will be returned. The Return IOPB will also report whether any commands "In Progress" were flushed from the Work Queue. Flushing an "In Progress" command may require a SCSI bus reset to properly clear the effects of the command out of the Target. If the Reset SCSI Bus on Command In Progress (RIP) bit is not set in the Options Word of the Flush Work Queue IOPB, it is up to the host to explicitly issue a SCSI Reset command to the Jaguar. This resets the SCSI bus in the event any In Progress commands are flushed.

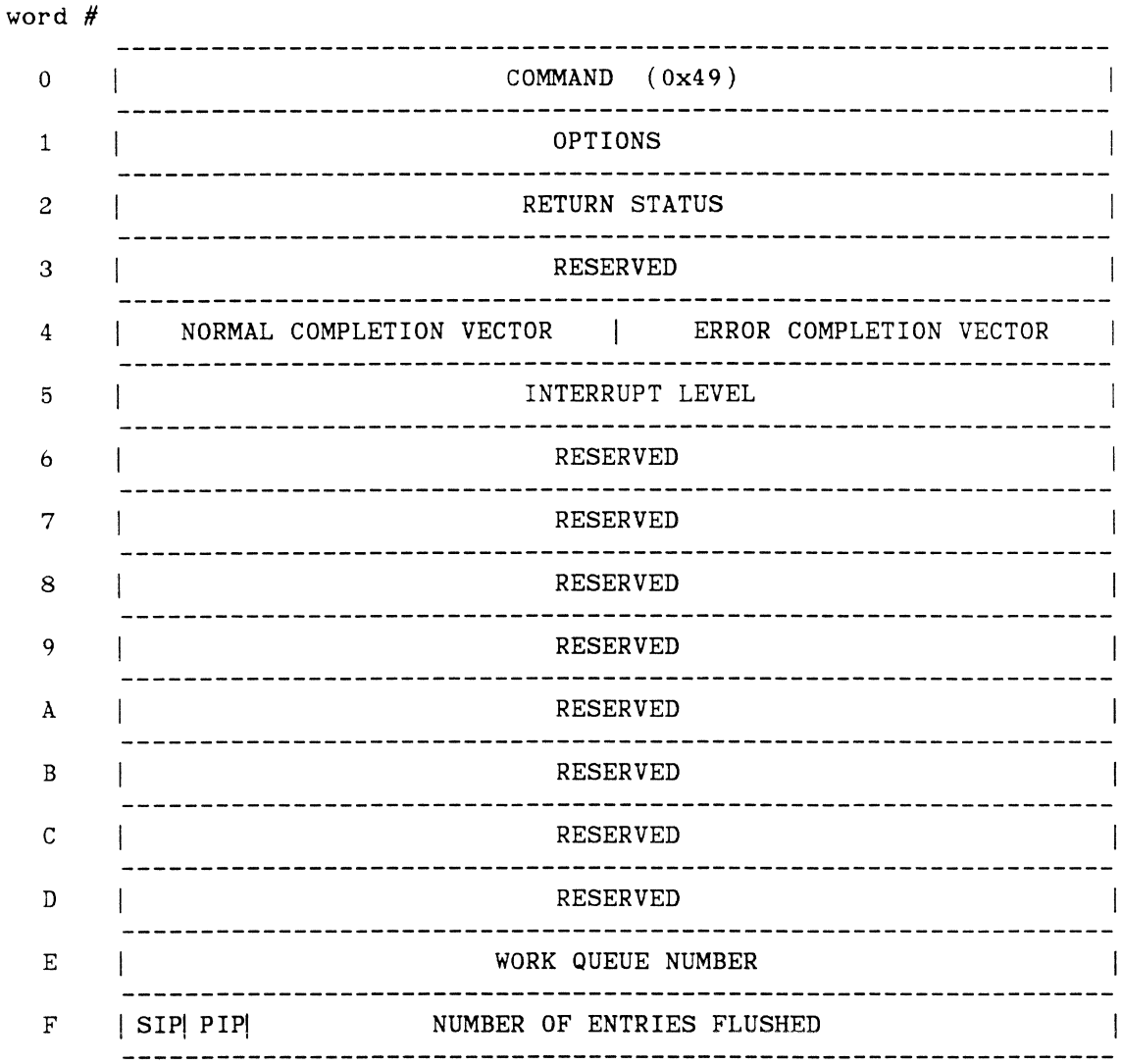


Figure 62. Flush Work Queue Command

The following section describes the function of each field in the Flush Work Queue IOPB. If the field is used as defined in IOPB Format, no additional description is provided.

Command (2 bytes):

The command code for the Flush Work Queue command is 0x49.

Options (2 bytes):

The host can enable the Jaguar to report each command that is flushed with a Command Complete Interrupt and an Error Status. If this option is not selected, the only interrupt the Jaguar will generate will be at the completion of the Flush Work Queue command.

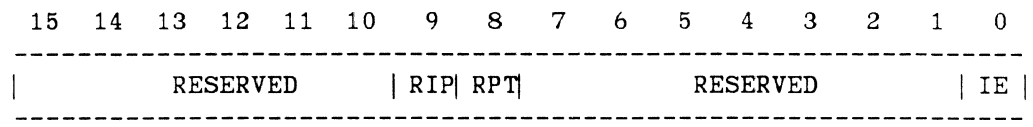


Figure 63. Work Queue Options

Bit 0 Interrupt Enable (IE):

Bits 1-7 Reserved:

These bits are reserved and must be set to a '0' by the host.

Bit 8 Report Flushed Commands (RPT):

When set to '1', the Report Flushed Commands bit enables the Jaguar to report each command after it is flushed. When set to a '0', the Jaguar interrupts only once at the completion of the Flush Work Queue command.

Bit 9 Reset SCSI Bus on Command In Progress (RIP):

The Reset SCSI Bus on Command In Progress bit enables the Jaguar to reset the SCSI bus when an In Progress command is flushed.

Bits 10-15 Reserved:

These bits are reserved and must be set to '0' by the host.

Work Queue Number (2 bytes):

This is the number of the work queue to be flushed. The host can also flush all of the work queues and the Command Queue by setting the Flush Queue bits in the Master Control Register (see Master Control Register).

Number of Entries Flushed/Flushed In Progress Command (2 bytes):

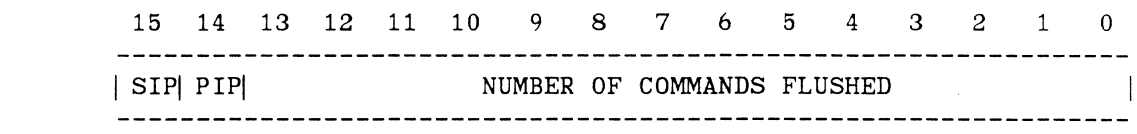


Figure 64. Number of Entries Flushed/In Progress Command Flushed

Bits 0-13 Numbers of Entries Flushed:

This is the number of entries that were flushed from the work queue.

Bit 14 Primary Bus Command In Progress (PIP):

The Jaguar sets this bit in the returned IOPB when an In Progress command is flushed on the primary SCSI bus. There can never be more than one In Progress command for any one work queue, but because the SCSI bus allows Targets to disconnect, there can be multiple In Progress commands on each SCSI bus.

Bit 15 Secondary Bus Command In Progress (SIP):

The Jaguar sets this bit in the returned IOPB when an In Progress command is flushed on the secondary SCSI bus.

APPENDIX A

HARDWARE CONFIGURATION

There are five hardware configurable options on V/SCSI 4210 Jaguar boards:

1) the Short I/O address
2) the default Primary SCSI Bus ID
3) SCSI Termination
4) SCSI Terminator Power
5) the Bus Request Level

The Short I/O address and the default Primary SCSI Bus ID are programmed via Switch 1 (SW1) on the board. The Bus Request Level is set using jumper blocks JA4, JA5, and JA6.

The Short I/O address is set with switches 4 through 8 of SW1. The MSB is set with Switch 8 and the LSB is set with Switch 4. These six switches set the address to any 2K boundary in the Short I/O space. A switch in the ON or CLOSED position is set to logic '0'. A switch in the OFF or OPEN position is set to logic '1'.

Switch 8 is used to select the address modifiers for the V/SMD 4210 Short I/O space. If Switch 8 is on, only supervisor accesses are permitted (address modifier 2D only). If Switch 8 is off, then both 2D and 29 address modifiers are selected.

The following figure illustrates a switch setting for a starting address of 8800.

	ADDRESS	SHORT I/O ADDRESS					PRIMARY SCSI		
ADDRESS BIT	MOD	A15	A14	A13 MSB	A12	A11 LSB	BUS ID		
SWITCH #	9	8	7	6	5	4	3	2	1
POSITION	OFF	OFF	ON	ON	ON	OFF	X	X	X
VALUE	2D/29	8	4	2	1	8	4	2	1

Figure A1. SW1 Switch Setting

The default Primary SCSI Bus ID used by the Jaguar is set with switches 1 through 3 of SW1. Switch 3 is the MSB and Switch 1 is the LSB. A switch in the ON or CLOSED position is set to logic '0'. A switch in the OFF or OPEN position is set to logic '1'.

Bus Request priority level can be selected from '0' (lowest priority) to '3' (highest priority) using jumper blocks JA4, JA5, and JA6. All of the possible jumper configurations for Bus Request priorities are illustrated on the following page.

V/SCSI 4210 PRODUCTS

V/SCSI 4210-0-SE	Jaguar	Full P2, Single-ended drivers. Cannot be converted to differential.
V/SCSI 4210-1-SE	Jaguar	B row only, Single-ended drivers. Cannot be converted to differential.
V/SCSI 4210-2-DF	Jaguar	Full P2, Differential drivers. Cannot be converted to single-ended.
V/SCSI 4210-DC-SE		SCSI daughter card, Single-ended drivers. Can be used with any mother card above. Cannot be converted to differential.
V/SCSI 4210-DC-DF		SCSI daughter card, Differential drivers. Can be used with any mother card above. When used with V/SCSI 4210-2-DF, must use front panel for Daughter connections (there are not enough pins on P2). When used with V/SCSI 4210-3-DF or V/SCSI 4210-1-SE, must use front panel for Daughter connections. Cannot be converted to single-ended.
V/SCSI 4210-PB		P2 Adapter Card

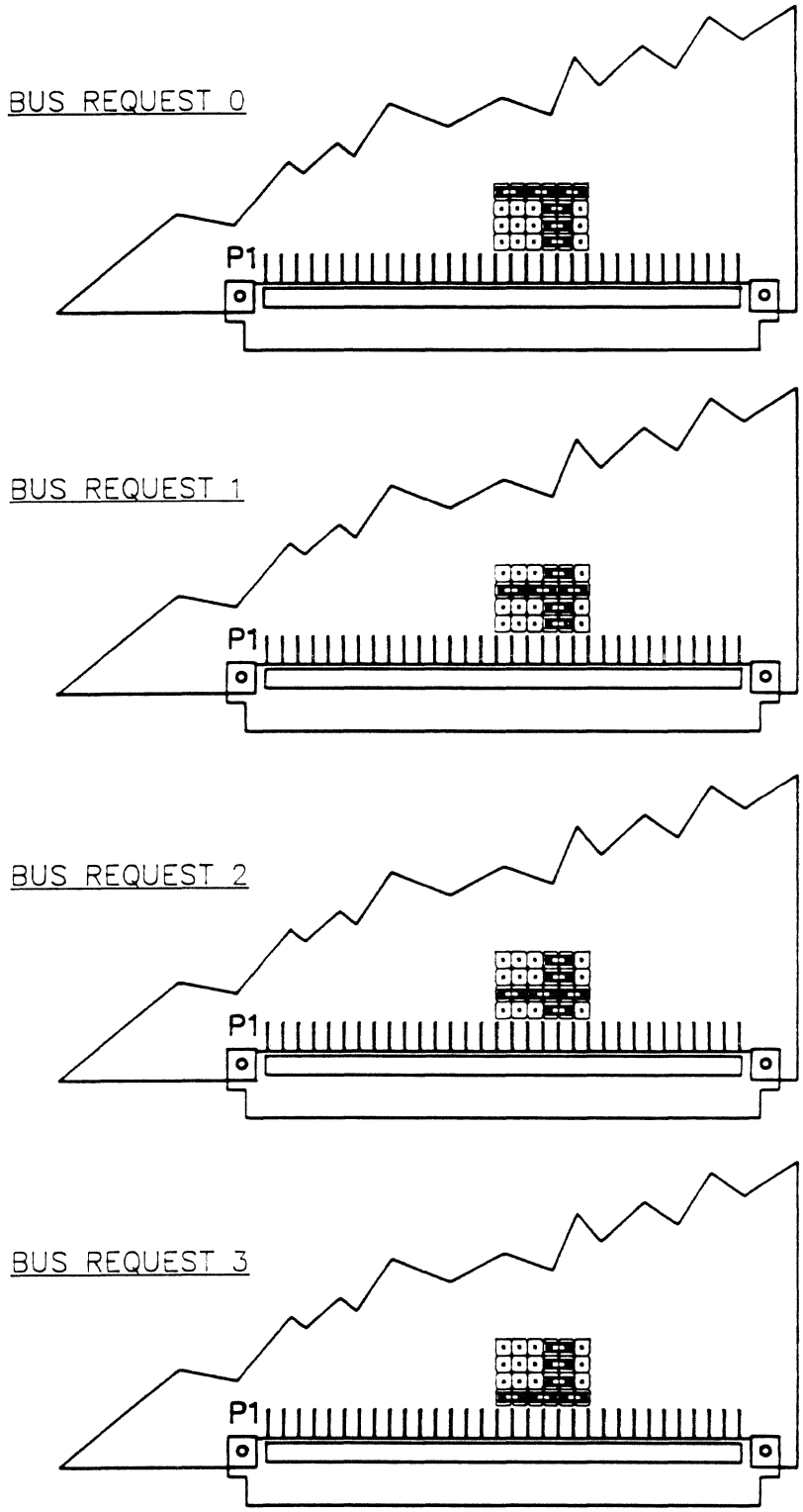


Figure A2. Bus Request Jumpers

JA1	This jumper connects Terminator Power to the SCSI Bus. JA1 is located next to P4, the secondary SCSI Bus Connector. This jumper is not installed at the factory.
F1 - FUSE	This fuse protects the SCSI Terminator Power when provided by the Jaguar. The fuse is a Littlefuse PN 251001.
SCSI TERMINATION	RN1, RN2 and RN3 provide termination for the primary SCSI Bus when installed. When the Jaguar is not at one end of the cable, these resistor sips should be removed. Termination is installed at the factory.
	The jumpers listed below are for factory use and should not be changed.
JA2 and JA3	These two jumpers are for oscillator testability. Both must be in place for proper Jaguar operation.
JA4	This jumper is used to select the EPROM size. It is set at the factory and should not be moved.
1-2	64K byte EPROM (27512)
2-3	32K byte EPROM (27256) Factory Setting

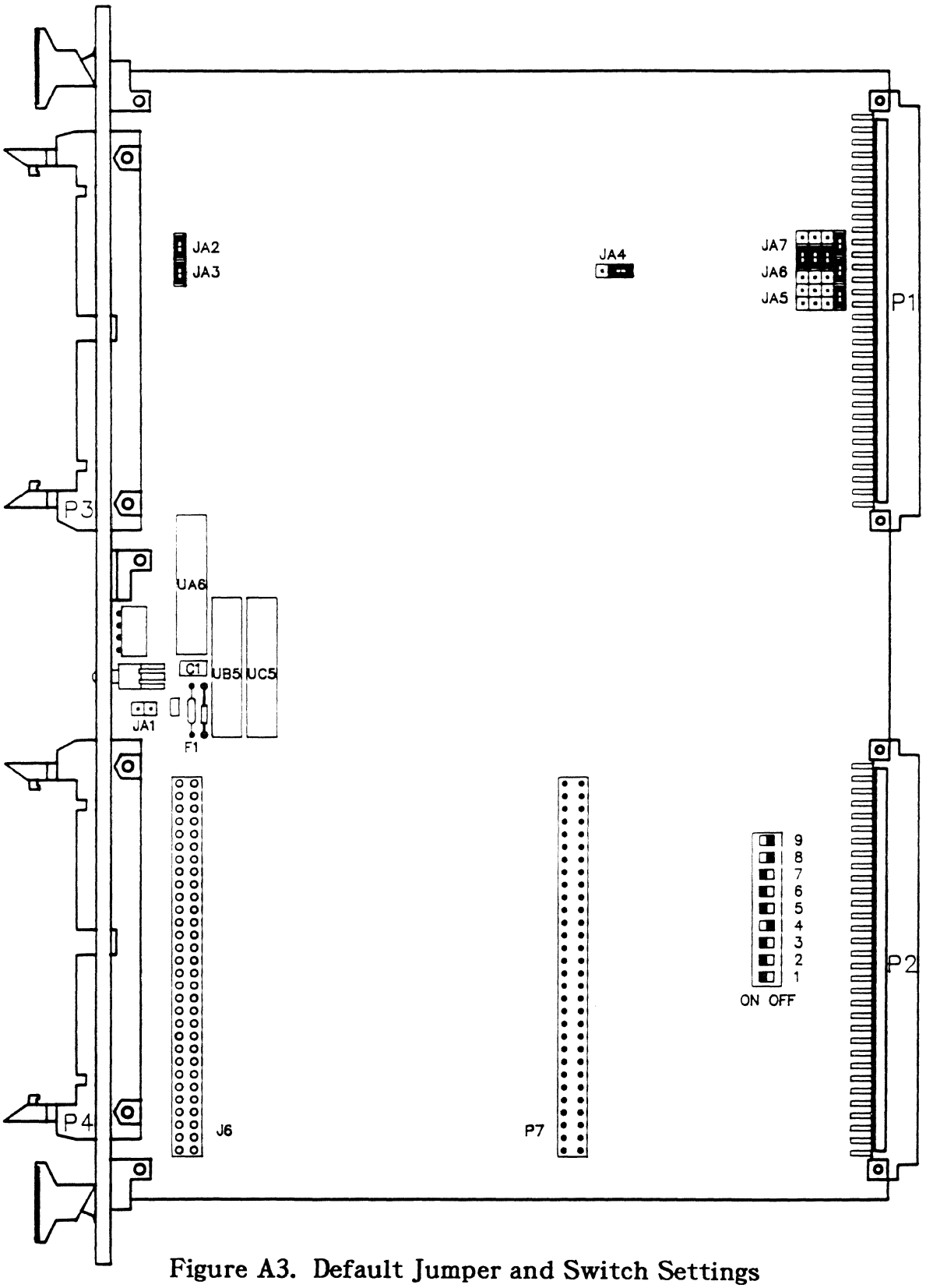


Figure A3. Default Jumper and Switch Settings

DAUGHTER BOARD HARDWARE CONFIGURATION

There are three hardware configurable options on the V/SCSI 4210 Jaguar daughter boards:

1) the default Secondary SCSI Bus ID
2) the SCSI Termination
3) the SCSI Terminator Power

The default Secondary SCSI Bus ID is set by jumpers JA1 through JA3. SCSI Termination is provided by the three 8-pin sips at the edge of the board. SCSI Terminator Power is selected with jumper JA4. (See Figure A4).

JA1 - JA3 JA1 through JA3 select the default SCSI Bus ID of the secondary port. JA3 is the most significant bit of the address and JA1 is the least significant bit. No jumper installed selects a '0' for that bit. Installing the jumper selects a '1' for that bit. Jumpers are not installed at the factory, therefore, the default selection is SCSI Address 0.

JA4 Installing a jumper at JA4 connects the Secondary Port to SCSI Terminator Power. No jumper is installed on JA4 at the factory.

SCSI Termination The three 8-pin sips at the edge of the card provide SCSI Termination and should be supplied if the Jaguar is at either end of the SCSI cable. The termination is installed at the factory.

V/SCSI 4210-PB P2 ADAPTER CARD

There are no jumpers or switch settings on this board. (See Appendix E).

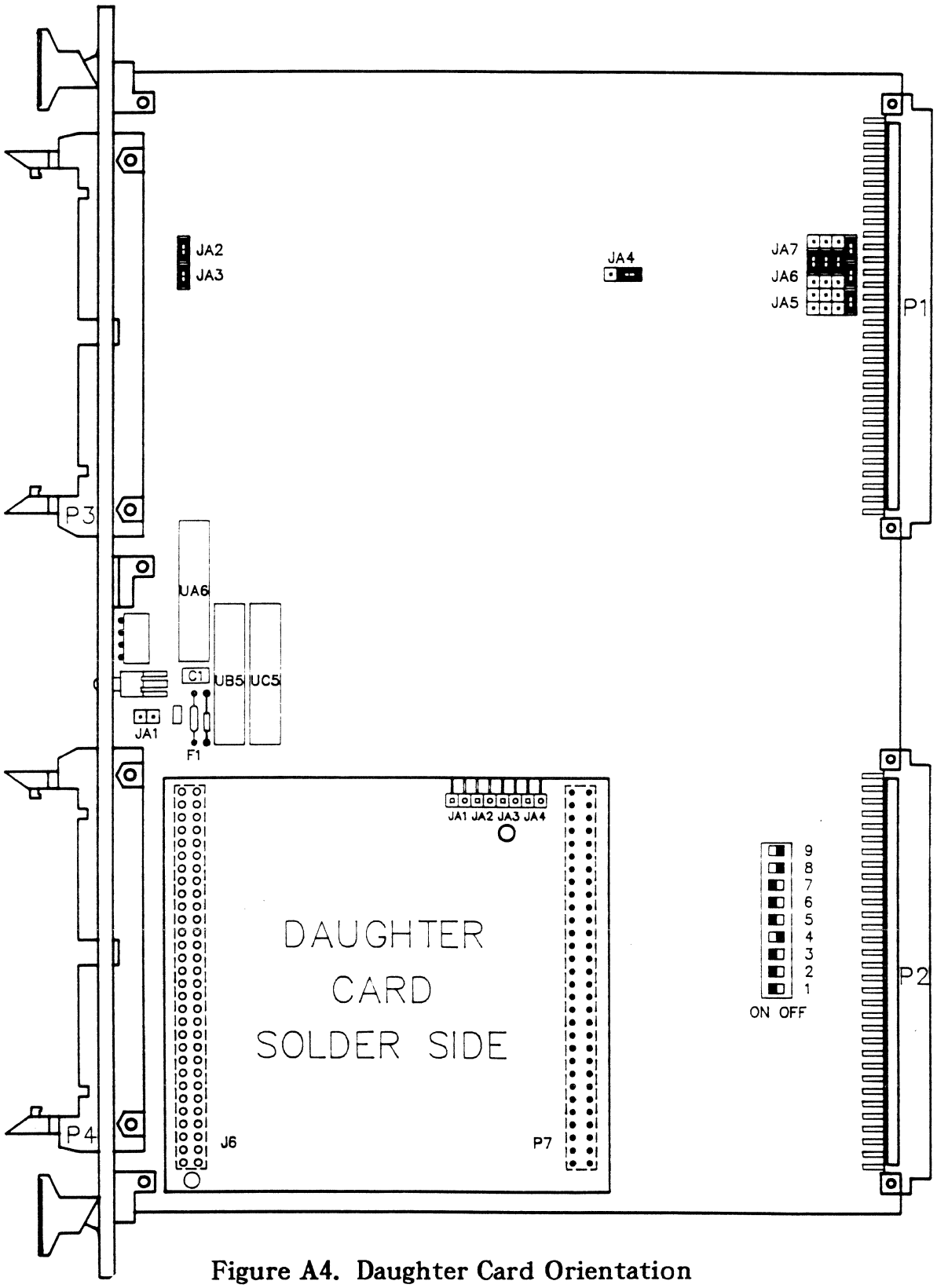


Figure A4. Daughter Card Orientation

VME P2 Pin	SCSI P3 Pin	SCSI SIGNAL NAME Single Ended
	1	GND
C32	2	DB0–
	3	GND
C31	4	DB1–
	5	GND
C30	6	DB2–
	7	GND
C29	8	DB3–
	9	GND
C28	10	DB4–
	11	GND
C27	12	DB5–
	13	GND
C26	14	DB6–
	15	GND
C25	16	DB7–
	17	GND
C24	18	DBP–
--	19	GND
--	20	GND
--	21	GND
--	22	GND
--	23	GND
--	24	GND
--	25	NC
C21	26	TERMPWR
--	27	GND
--	28	GND
--	29	GND
--	30	GND
--	31	GND
C17	32	ATN–
--	33	GND
--	34	GND
--	35	GND
C15	36	BSY–
--	37	GND
C12	38	ACK–
--	39	GND
C10	40	RST–
--	41	GND
C8	42	MSG–
--	43	GND
C6	44	SEL–
--	45	GND
C4	46	C/D–
--	47	GND
C2	48	REQ–
--	49	GND
C1	50	I/O–

Figure A5. Pin-Out for the V/SCSI 4210 Jaguar SCSI Port (See Figure A4.)

Example on reading this figure:

Single-ended SEL signal can be found on P2, Row C, Pin 6 or on P3, Pin 44.

VME P2 Row/Pin	SCSI P4 Pin	SCSI SIGNAL NAME Single Ended
A32	1	GND
A22	2	DB0–
A31	3	GND
A21	4	DB1–
A30	5	GND
A20	6	DB2–
A29	7	GND
A19	8	DB3–
A28	9	GND
A18	10	DB4–
A27	11	GND
A17	12	DB5–
A26	13	GND
A16	14	DB6–
A25	15	GND
A15	16	DB7–
A24	17	GND
A14	18	DBP–
C23	19	GND
A13	20	GND
C22	21	GND
––	22	GND
––	23	GND
––	24	GND
C20	25	NC
A12	26	TERMPWR
––	27	GND
––	28	GND
C18	29	GND
A11	30	GND
––	31	GND
A10	32	ATN–
C16	33	GND
A9	34	GND
C14	35	GND
A8	36	BSY–
C13	37	GND
A7	38	ACK–
C11	39	GND
A6	40	RST–
C9	41	GND
A5	42	MSG–
C7	43	GND
A4	44	SEL–
C5	45	GND
A3	46	C/D–
C3	47	GND
A2	48	REQ–
––	49	GND
A1	50	I/O–
C19	––	NC
A23	––	NC

Figure A6. Pin-Out for the Optional Second SCSI Port (See Figure A4.)

Example on reading this figure:

Single-ended SEL signal can be found on P2, Row A, Pin 4 or on P4, Pin 44.

APPENDIX B

CONTROLLER ERROR CODES

The Jaguar Controller Error Codes field returns information pertaining to the operation of the IOPB returned in the Command Response Block. Statuses have been separated into five groups: MACSI/Controller, General, Error Recovery, VME, and SCSI errors. The V/SCSI 4210 Jaguar controller status definitions are reported in hexadecimal format.

MACSI/CONTROLLER ERROR CODES

Hex Code Description

0x00 GOOD STATUS:

The controller has completed the command and no errors were detected. The Pass-Back status field contains the Pass-Through status.

0x01 QUEUE FULL:

The work queue specified for this command is full and cannot receive another entry. The command is not executed and is moved directly to the Command Response Block Queue with this status set. The queue can receive another entry after a currently active command has completed or if the queue is flushed.

0x02 WORK QUEUE INITIALIZATION ERROR:

The work queue specified has not been initialized. The command is not executed and is moved directly to the Command Response Block Queue with this status set. The Work Queue should be initialized with an Initialize Work Queue Command.

0x03 **FIRST COMMAND ERROR:**

The first command sent to the board was not an Initialize Controller command. The board should be reset and the first command issued should be the Initialize Controller command in order to set up the MACSI operating parameters.

0x04 **COMMAND CODE ERROR:**

The command field contains an invalid command type. Either a SCSI IOPB type or a Control IOPB type must be specified.

0x05 **QUEUE NUMBER ERROR:**

The work queue number specified in the CQE is invalid. Valid work queue numbers are 0 to 14.

0x06 **QUEUE ALREADY INITIALIZED:**

The work queue specified to be initialized has already been initialized. To re-initialize a queue, set the IWQ bit in the options field.

0x07 **QUEUE UN-INITIALIZED:**

An IOPB was issued to a work queue that has not been initialized. Work queues must be initialized with operating parameters before usage.

0x08 **QUEUE MODE NOT READY:**

The Start Queue Mode bit was set before the Initialize Controller Command was issued. The Initialize Controller Command should be the first board operation after power up to configure the MACSI interface.

0x09 **COMMAND UNAVAILABLE:**

The IOPB type specified has not been implemented in the current firmware.

0x0A **PRIORITY ERROR:**

The priority specified for the work queue is invalid.

GENERAL ERROR CODE INFORMATION

Hex Code	Description
0x10	**RESERVED FIELD ERROR:**
	A reserved field in the IOPB has non-zero data in it.
0x11	**RESET BUS STATUS:**
	The SCSI Reset IOPB has executed successfully and generated a Reset on the bus.
0x12	**PORT 2 UNAVAILABLE:**
	An IOPB has been issued to Port 2 but the port is not installed.
0x13	**SCSI ID ERROR:**
	The SCSI device ID requested is invalid because of a conflict with the Jaguar device ID. All devices on the bus require unique SCSI IDs.
0x14	**SCSI BUS RESET STATUS:**
	The command could not execute because the SCSI bus is held in the reset state. This may be caused by an un-powered device on the bus, improper termination, or an inverted cable.
0x15	**COMMAND ABORTED BY RESET:**
	The command has been aborted due to a SCSI reset condition received during execution of the command.

VME ERRORS

Hex Code	Description
0x20	**VME BUS ERROR:**
	This error indicates that a bus error occurred during the DMA transfer of the data to or from the buffer or the bus.

0x21 **VME TIME OUT:**

This error indicates that bus acquisition was not completed within the programmed time out period. This error is typically caused by a nonexistent address or address modifier in the IOPB.

0x23 **VME ILLEGAL ADDRESS:**

For 16-bit transfers, the starting address of the VME buffer must fall on a word boundary (even address). For 32-bit transfers, the starting address of the VME buffer must fall on a long word boundary (multiple of 4).

0x24 **VME ILLEGAL MEMORY TYPE:**

An illegal memory type has been specified.

0x25 **ILLEGAL COUNT SPECIFIED**

The maximum transfer length specified is not an even number. All transfer counts must be even since the controller can only perform word or long word transfers. If an odd count is to be transferred across the SCSI bus, the count specified in the maximum length field must be padded by '1' to round up the VME transfer count to a word or long word multiple.

SCSI ERRORS

Hex Code Description

0x30 **SCSI SELECTION TIME OUT ERROR:**

The selection phase of the SCSI device has failed. The error may occur due to an incorrect Target ID.

0x31 **SCSI DISCONNECT TIME OUT ERROR:**

A disconnected device has not re-selected the board in the time out period. This may be caused by a hardware error, or a command that may take a very long period of time to execute.

0x32 **SCSI ERROR:**

The SCSI operation did not complete successfully due to a hardware error or an abnormal operation sequence.

0x34 **SCSI TRANSFER COUNT EXCEPTION:**

The SCSI Transfer Count of Data did not match the count specified in the maximum count length field. The amount of data actually transferred on the SCSI bus will be returned in the maximum count length field. This status may not be considered an error for commands that intentionally allocate more buffer than the SCSI command uses.

ERROR HANDLING CODES

Hex Code Description

0x80 **FLUSH ON ERROR IN PROGRESS:**

This status is set when the IOPB is flushed because an error condition has occurred and the work queue has the abort enable option set. This causes all queued IOPBs to be flushed until the abort acknowledge has been received.

0x81 **FLUSH WORK QUEUE STATUS:**

The queued IOPB is being flushed in response to a Flush Work Queue Command.

APPENDIX C

SCSI DEVICE ERROR HANDLING

A SCSI Device Error is defined to be the completion of a SCSI Command with a status byte of any value other than '0'. Since a device may have many commands queued for it at the time an error occurs, it is desirable for the host to have a mechanism of altering the command execution order after an error. Depending on the application, there may be a number of ways to accomplish error handling. The Jaguar provides two simple features that should be capable of all error handling needs.

The features are called Freeze Work Queue on Error and Abort Work Queue on Error. The option is enabled at work queue initialization time and is active on a work queue independent of the other work queues.

FREEZE WORK QUEUE OPTION USAGE ON JAGUAR

The Freeze Work Queue option provides a mechanism for freezing the state of a work queue when an error occurs. Error handling can be accomplished by using Work Queue 0. After the error handling has been completed, the work queue can be unfrozen. This option is probably the only method needed to handle SCSI device errors.

This mechanism uses the Freeze Work Queue Option Bit located in the Work Queue Options field of the Initialize Work Queue IOPB. The bit is initialized on a per queue basis during the Work Queue Initialization command. When enabled, the Freeze Enable bit will halt all further commands to a device when a Pass-Back status other than good status (00) is received from that device. The queue is not frozen for controller errors. The queue's state is frozen to allow the error handling sequence to occur before resuming normal command execution. This error handling sequence may include commands issued to the failing device through the MCE (usually a SCSI request sense command). After the condition has been cleared, the queue can be unfrozen by use of the Thaw bit in the MCSB.

Execution of commands in the frozen queue is restarted by setting the least significant bit of the Thaw Work Queue Register.

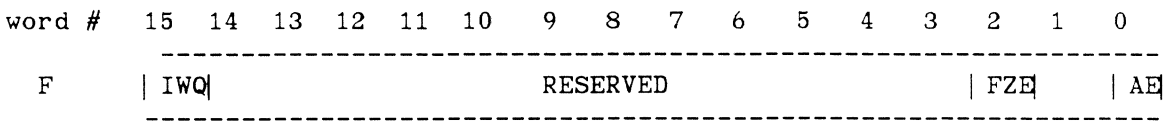


Figure C1. Work Queue Options

The Freeze Enable bit (FZE) is set during the Work Queue Init command. This attribute will be in effect for that queue only. All commands that do not return a good status will freeze the queue. When the host sees a command return from a work queue that has Freeze on Error enabled with a SCSI device error, the host must unfreeze (thaw) the work queue after taking the error handling steps needed for that particular error.

The frozen work queue is unfrozen by selecting that work queue number in the Thaw Queue Register and then setting Bit 0 of that register. The Jaguar will clear the register to acknowledge the thawing of the work queue. The Thaw Work Queue Status Register is located in the fourth word of the Master Control/Status Block and is defined as follows:

MASTER CONTROL/STATUS BLOCK

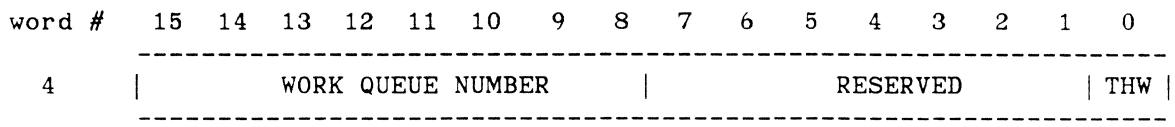


Figure C2. Thaw Work Queue Register

COMMENTS ON FREEZE WORK QUEUE ON ERROR USAGE

Work Queue 0 does not have Freeze Work Queue on Error enabled. This is not needed as Work Queue 0 has a length of one.

There is no indication to the host that a work queue is frozen other than the completion of a Pass Through command with a Pass-Back status not equal to '0'. The work queue will remain frozen until it is thawed.
Commands sent to a work queue that is frozen will not be executed until the work queue is unfrozen.

ABORT WORK QUEUE ON ERROR

The Abort Work Queue on Error option is generally less useful than the Freeze Work Queue on Error option. This option causes the Jaguar to abort all commands for that work queue until a command is issued with the Abort Acknowledge bit set to '1' in the command's Queue Entry Control Register.

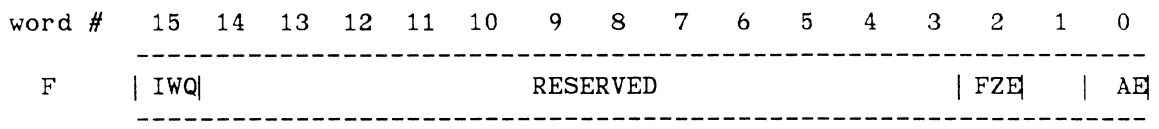


Figure C3. Work Queue Options

Abort Enable is specified by setting Bit 0 of the Work Queue Option field in the Initialize Work Queue command. The option is in effect only in the work queue being initialized.

When a SCSI Device error occurs, the failing IOPB will be returned with the bad Pass-Back status. All other commands for that work queue will be returned with a Command Complete and Abort Queue set to '1' in the Command Response Word. This will continue until a command is found with the Abort Acknowledge bit set to a '1' in the commands' Queue Entry Control Register. Note that this means not just the commands presently in the Work Queue, but all commands for that Queue will be aborted until the Abort is acknowledged.

APPENDIX D

SCATTER/GATHER

The Scatter/Gather option allows the user to place contiguous peripheral data in non-contiguous areas of system memory (scatter operation) or to place non-contiguous areas of system memory in contiguous areas of the peripheral (gather operation).

The purpose of the Scatter/Gather option is to unburden the host of having to process several transactions when non-contiguous blocks of data are to be transferred. The option allows multiple blocks of data to be transferred using only one command, rather than one command per block. So, whenever the Scatter/Gather option is used, system performance is improved because both the number of VMEbus interrupts and the number of bus transactions associated with common peripheral activity are minimized.

The Scatter/Gather operation is enabled by setting the S/G bit in the options field of the Pass-Through IOPB. Setting this bit makes the Buffer Address field point to the Scatter/Gather List, which describes the format of the VME transfers. Lists can reside anywhere in system memory but, for optimum performance, they should be stored in Jaguar Short I/O. If the list resides in Short I/O, the memory type field in the IOPB should be set to '3'. If the list resides in system memory, the memory type should be set for either 16- or 32-bit transfers.

USING SCATTER/GATHER

Setting Bit 1 of the Pass-Through command options field enables Scatter/Gather.

word #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	RESERVED														S/G	IE

Figure D1. Pass-Through Options

With Scatter/Gather enabled, the Memory Type/Address Modifier, Buffer Address, and Transfer Length fields reference the Scatter/Gather Element List instead of the data for the command.

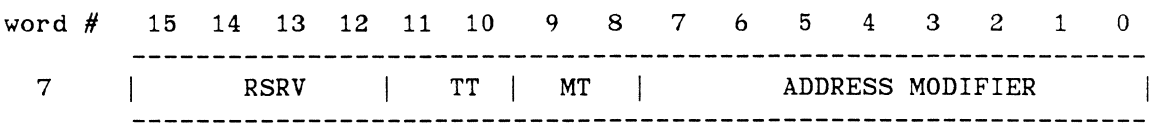


Figure D2. Memory Type/Address Modifier

MEMORY TYPE (MT)	0	Reserved
	1	16-Bit Access to Scatter/Gather List
	2	32-Bit Access to Scatter/Gather List
	3	Scatter/Gather List Resides in Short I/O

Memory Type has a memory type not supported for non-Scatter/Gather. A '3' allows the Scatter/Gather List to reside in the Short I/O space of the Jaguar. In this case, the address modifier is not used and should be cleared to '0'.

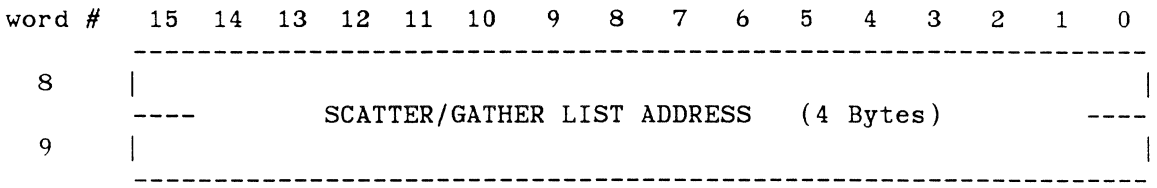


Figure D3. Scatter/Gather List Address

When Scatter/Gather is used, the Buffer Memory Address field is used to point to the Scatter/Gather List. If Memory Type is 3, the Scatter/Gather List Address is an offset from the base address of the Short I/O. Otherwise, it contains the system memory address of the Scatter/Gather List.

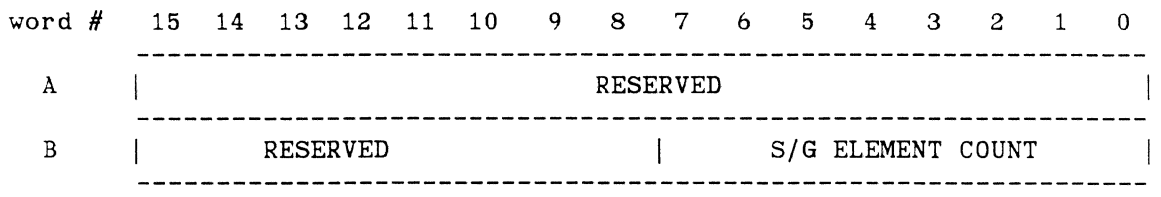


Figure D4. Scatter/Gather Element Count

The Entry count contains the number of elements in the Scatter/Gather List. Valid Counts are 1 to 64.

Scatter/Gather requires an additional field that is used for the transfer count of the data used in the command.

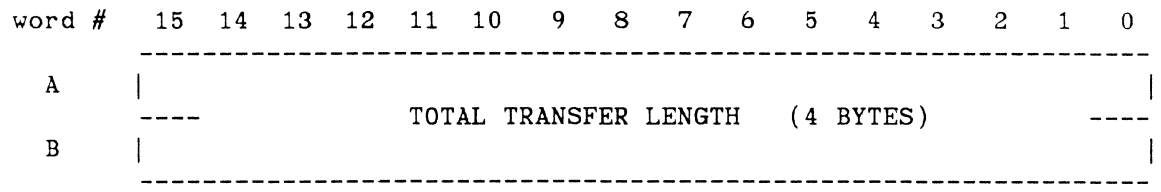


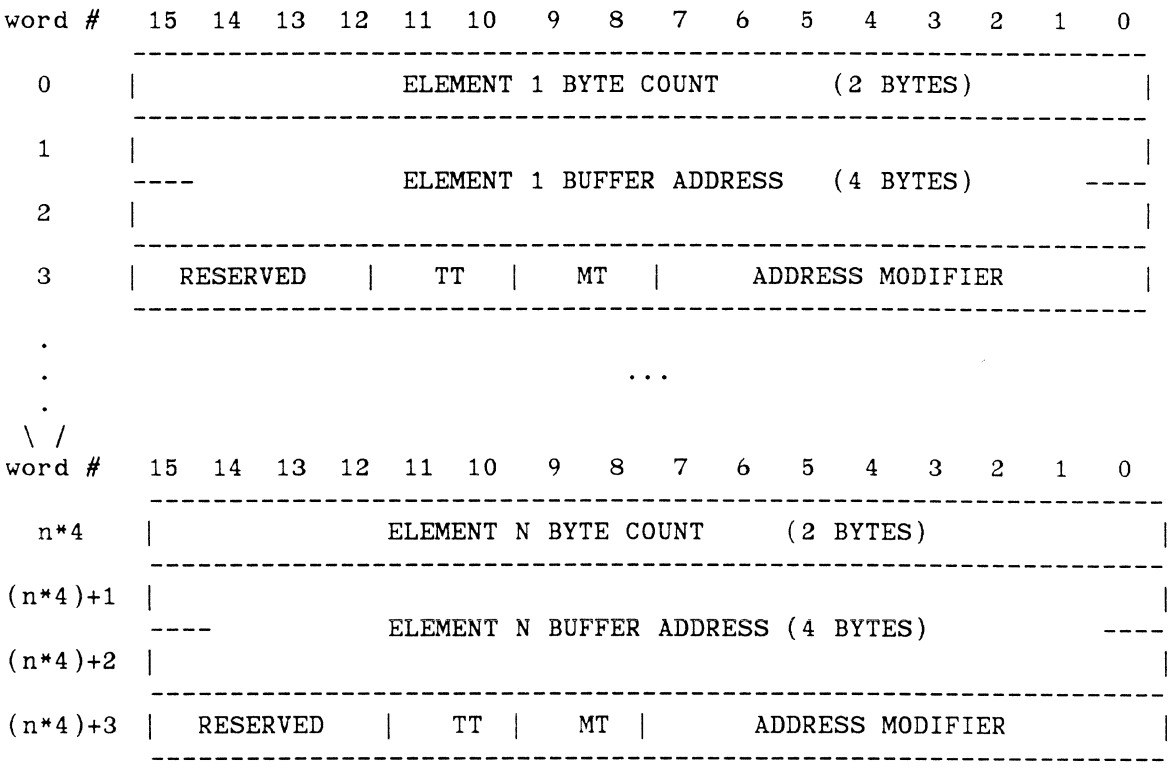
Figure D5. Total Transfer Count

The Total Transfer Length is the sum of the individual element entry counts. If this field is '0', the controller will calculate this value internally. A '0' value is provided for compatibility with early firmware revisions. All new applications should provide the Total Transfer Count.

SCATTER/GATHER LIST

The Scatter/Gather option uses a list of elements to control the Scatter/Gather operation. Each element in the list specifies the byte count, address, memory type, and address modifier for each block of data in system memory that is to be transferred by one SCSI Pass-Through command.

Each element in the list is an 8-byte entry. The format is as follows:


word # 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 ELEMENT 1 BYTE COUNT (2 BYTES)
1
ELEMENT 1 BUFFER ADDRESS (4 BYTES)
2
3 RESERVED TT MT ADDRESS MODIFIER
...
word # 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
n*4 ELEMENT N BYTE COUNT (2 BYTES)
(n*4)+1
ELEMENT N BUFFER ADDRESS (4 BYTES)
(n*4)+2
(n*4)+3 RESERVED TT MT ADDRESS MODIFIER

D6. Scatter/Gather Element List Format

This Scatter/Gather List can have from 1 to 64 elements. Using Scatter/Gather for lists with just one element, however, would be inefficient.

APPENDIX E

V/SCSI 4210-PB P2 ADAPTER CARD

The V/SCSI 4210-PB P2 Adapter Card converts the VMEbus P2 pin-out of the Jaguar to standard SCSI connectors. The physical dimensions of this card is 98 mm by 53 mm. Two standard 50-pin ribbon cable connectors are provided. The Jaguar supports either two single-ended interfaces or one single-ended interface and one differential interface. P4 can only be used for the single-ended interface. P3 may be used for the single-ended interface or the differential interface. This depends on the configuration of the mother board and the daughter board.

A schematic of the V/SCSI 4210-PB P2 Adapter Card is provided on the next page to clarify the connection from the Jaguar mother board VMEbus P2 connector to the SCSI 50-pin connectors.

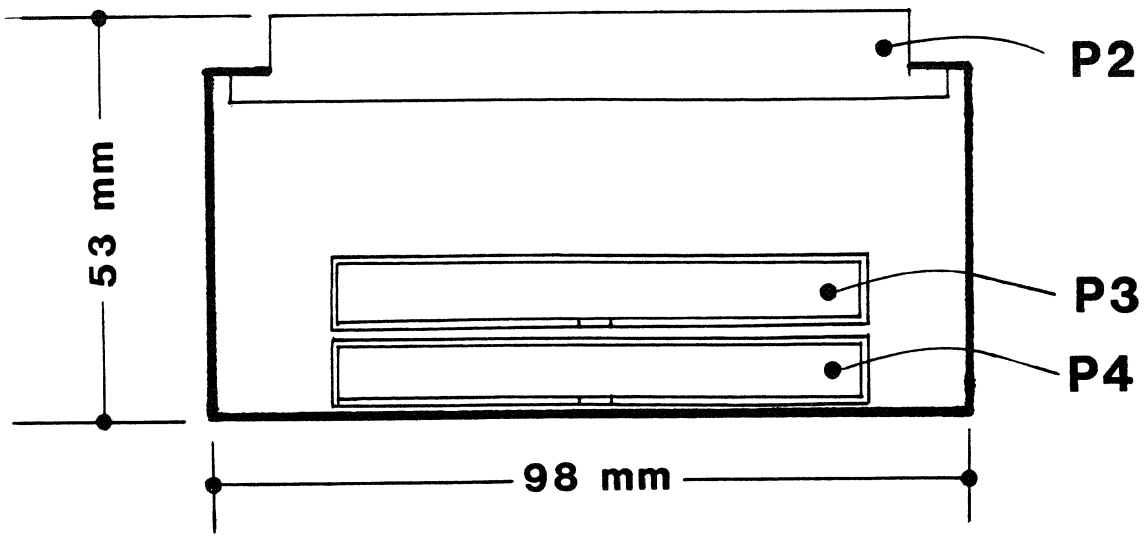


Figure E1. V/SCSI 4210-PB P2 Adapter Card

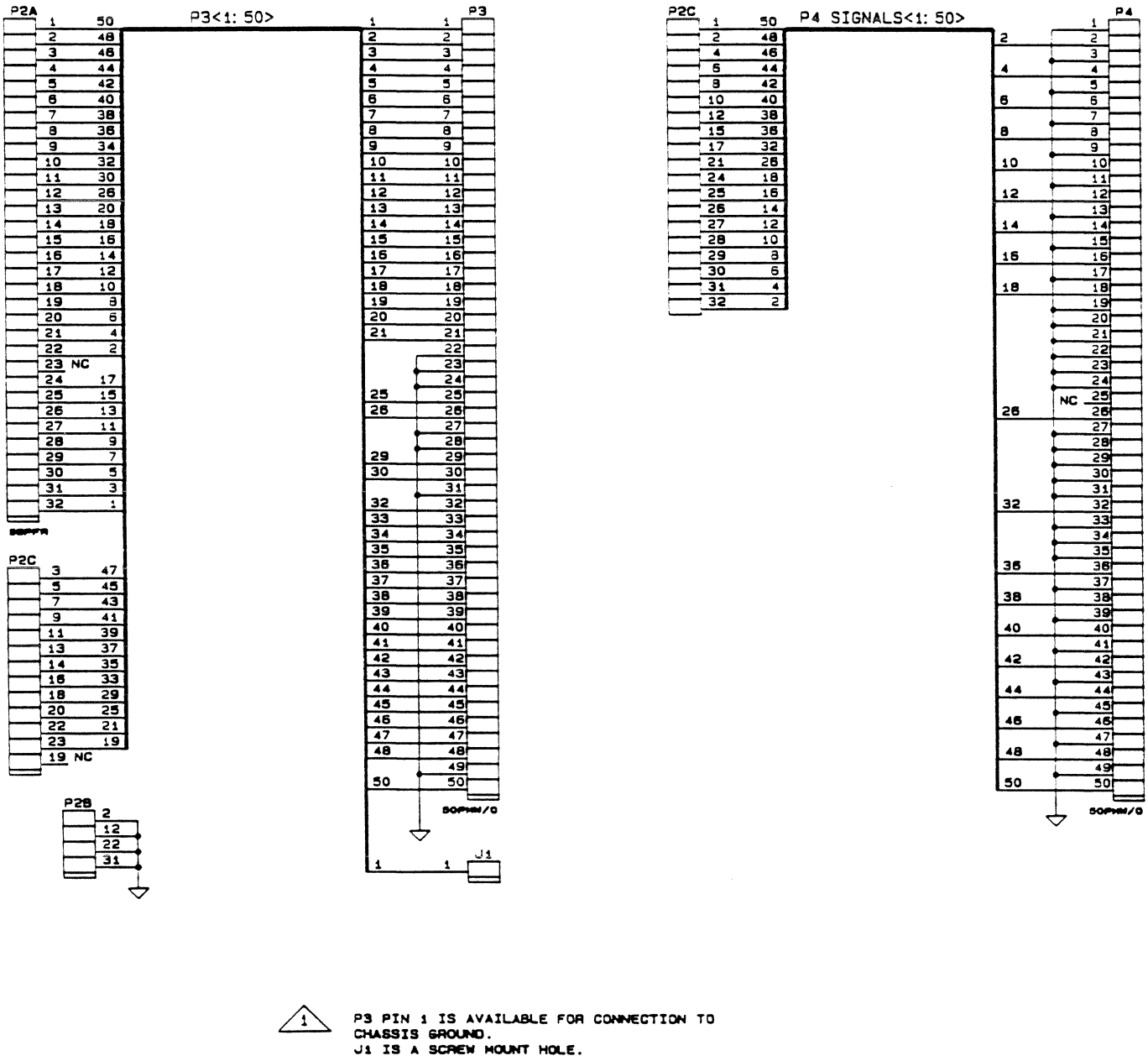


Figure E2. V/SCSI 4210-PB P2 Adapter Card Schematic

GLOSSARY

AA	Abort Acknowledge
AE	Abort Enable
AM/MT/TT	Address Modifier/Memory Type/Transfer Type
AQ	Abort Queue
BOK	Board OK
BUS	SCSI Bus Selection
CC	Command Complete
CIB	Controller Initialization Block
CIOPB	Control IOPB
CNA	Controller Not Available
CQ	Command Queue
CQ	Command Queue
CQA	Command Queue Entry Available
CQE	Command Queue Entry
CRB	Command Response Block
CRBV	Command Response Block Valid/Clear Interrupt
CRSW	Command Response Status Word
CSS	Controller Specific Space
DFT	Default
DIR	VME Transfer Direction
ER	Error
EX	Exception
EXT	Extended Addressing Enable
FLQ	Flush Queue
FLQR	Flush Queue and Report
FZE	Freeze Enable
GO	Go/Busy
HPC	High Priority Command
HUS	Host Usable Space
IE	Interrupt Enable
IL	Interrupt Level for the Interrupt on Queue Available
IOPB	Input/Output Parameter Block
IQAR	Interrupt on Queue Available Register
IQEA	Interrupt on Queue Entry Available
IQHE	Interrupt on Queue Half Empty Enable
IV	Interrupt Vector for Interrupt on Queue Available
IWQ	Initialize Work Queue
LUN	Logical Unit Number
LVL	Interrupt Level

MACSI	Multiple Active Command Software Interface
MCE	Master Command Entry
MCR	Master Control Register
MCSB	Master Control/Status Block
MSR	Master Status Register
MT	Memory Type
PIP	Primary Bus Command In Progress
QECR	Queue Entry Control Register
QFC	Queue Flush Complete
QMS	Queue Mode Started
RES	Reset Controller
RIP	Reset SCSI Bus on Command In Progress
RPT	Report Flushed Commands
RSRV	Reserved
SCSI ID	SCSI Device ID
SFEN	Sysfail Enable
SG	Scatter/Gather
SIP	Secondary Bus Command In Progress
SQM	Start Queue Mode
THW	Thaw Work Queue
TT	Transfer Type

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